Open access Journal International Journal of Emerging Trends in Science and Technology

Performance of Micro Controller Based Seven Level Diode Clamped Multilevel Inverter for Three Phase Induction Motor

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Abstract
This paper presents a micro controller based control of multilevel inverter for three phase Induction motor. Pulse Width Modulation (PWM) techniques; introduced three decades ago, are the most used methods to control the voltage and frequency supplied to electrical AC machines. Multilevel inverter has gained attention in recent years due to its high power capability associated with lower output harmonics. Several multilevel topologies have been reported in the literature and this paper focuses on Diode Clamped multilevel inverter built to implement the proposed conduction table with seven voltage levels. Gating signals an regenerated using P IC microcontroller. The performance of the inverter has been analyzed and compared with the result obtained from theory. A scheme based on 7-level PWM inverter, which control a high performance 8-bit standard microcontroller with gate driver circuit and additional hardware is used, which allows a flexible and economical solution. The output voltage can be varied in a large range and with a good resolution. Experimental data obtained from an induction motor drive will be presented and to check staircase sinusoidal waveform of line voltage on CRO.
Keywords: *Diode clamped multilevel inverter; Multicarrier SPWM technique; Microcontroller,*

Introduction

Multilevel voltage source inverter is recognized as an important alternative to the normal two levels voltage source inverter particularly in high voltage application. Using multilevel technique, the amplitude of the voltage is increased, stress in the switching devices is reduced and the overall harmonics profile is improved. Among the familiar topologies, the most popular one is cascaded multilevel inverter. It exhibits several attractive features such as simple circuit layout, less components counts, modular in organization and avoids. However as the number of output level increases, the circuit becomes bulky due to the increase in the number of power devices. In this project, it is proposed to employ a new technique to obtain a multilevel output using less number of power switches when compared to ordinary diode clamped multilevel inverter. The induction motor accepted in variable speed drives due to its distinguished advantages of easy construction as well as low cost machine. This asynchronous machine uses some internal parts that need maintenance or replacement. The control voltage applied to the asynchronous machine can transform the expression of electromagnetic torque of the asynchronous machine to practically the torque of the D.C. machine. In this work, the decoupling Vds and Vqs are used to control the flux particularly in the course of the component Ids and Iqs, which sharply to the suggestions of decoupling of the dependent excited D.C motor. The control of induction motor can transform the expression of

electromagnetic torque of to nearly the torque of the DC machine. Moreover, with multilevel inverter SPWM and application of rotor flux, the voltage applied to the Induction Motor (IM) solicits amodulator stage. This stage adds to the signal processing time and consequently limits the reactions of the control system, and hence the torque and speed response time. Also a hardware implementation of multilevel convertor with microcontroller control methodology for three phase induction motor system and its implementation in term of programming and code in real time operating system [5].

PWM Method

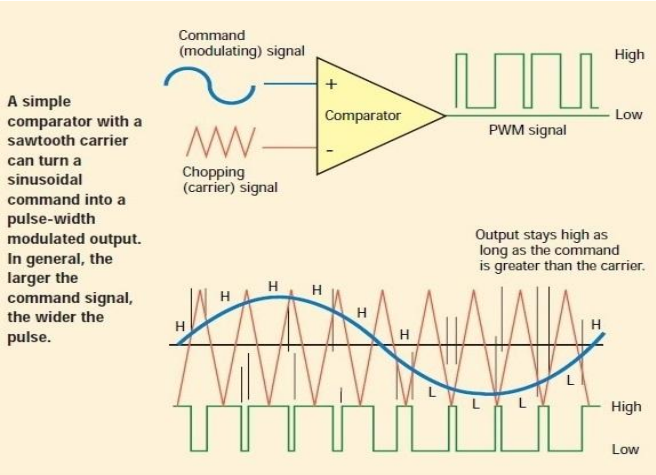

Figure.1 How to works PWM

The multilevel PWM inverters include an array of power semiconductors and capacitor voltage sources, output of which generate voltages in stepped waveform. The commutation of the switches allows the addition of the capacitor voltages which reaches the high voltage level at the output, while the power semiconductors withstand only with reduced voltage. A seven-level PWM inverter generates an output voltage with seven values (levels) with respect to the negative terminal of the capacitor. By considering that 'n' is the number of steps of the phase voltage with respect to the negative terminal of the inverter, then the number of steps in the voltage between two phases of the load 'K' is defined by:

$$K = 2m + 1 \ldots (1)$$

The number of steps P in the phase voltage of a single phase load in wyes connection is given by:

$$P = 2k + 1 \ldots (2)$$

The term multilevel starts with the three-level inverter. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveforms, it results to reduction in harmonic distortion. However, a high number of levels results in increasing the complexity and also introduce voltage imbalance problems [1].

Three different topologies have been proposed for multilevel inverters as diode-clamped (neutral clamped), capacitor-Clamped (flying capacitors) and cascaded multi cell with separate dc sources. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following: multilevel sinusoidal pulse width modulation (SPWM), multilevel selective harmonic elimination. The most attractive features of diode clamped multilevel inverters are as follows:

- It can generate output voltage with extremely low distortion.
- It draws input current with very low distortion.
- It generates smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, by using sophisticated modulation methods, CM voltages can be eliminated [8].
- They can operate with a lower switching frequency.

Seven Level DCMI

The early forms of DC to AC conversion are derived from the basic buck converter, where a power semiconductor is used to switch a DC signal into a square wave (Square Wave Inverter). With the introduction of power storage components, such as inductors and capacitors, this square wave will resemble a rough sinusoidal wave. The desired sinusoidal output can be further refined with the use of logic control on the semiconductors. It enables the positive and negative peaks of the square wave to be delayed (Phase Shifted Square Wave inverters), by creating a zero level. All these adjustment were made in the aid of producing a perfect sinusoidal output or in other words to

decrease the Total Harmonic Distortion (THD). The multilevel inverter with SPWM further refines the conversion of the DC input to an AC output. This advancement in inverter was not possible until recent semiconductor technology advancements. In this particular project, the semiconductors must have a high power rating combined with a high switching frequency. Multilevel inverters use high-speed semiconductor switches to switch the DC signal at varied time intervals, this will create varied pulse widths, hence the name Sinusoidal Pulse Width Modulator [6].

An *m*-level diode-clamped multilevel inverter typically consists of *m* – 1 capacitor on the dc bus and produces *m* levels of the phase voltage [18]. A three-phase seven-level structure of a DCMLI is shown in Figure.2 each of the three phases of the inverter shares a common dc bus, which has been subdivided by four capacitors into five levels. The voltage across each capacitor is *Vdc*, and the voltage stress across each switching device is limited to *Vdc*through the clamping diodes. Seven voltage levels can be obtained using six voltage sources and 36 diode and MOSFET switches.

Table.1 Number of components for 3ΦDCMLI

SR NO	Main Switches	Main Diodes	Clamping Diodes	DC Bus Capacitors	Total Numbers
1	6(N-1)	6(N-1)	3(N-1)(N-2)	3(N-1)	$3(N^2+2N-3)$

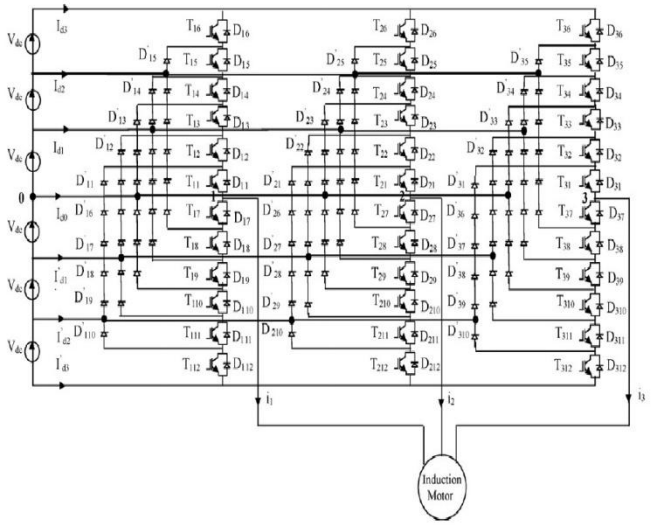

Figure.2 Three phase seven levels DCMI schematic

To produce a staircase-output voltage, consider three leg of the three-level inverter, as shown in Figure.2. The steps to synthesize the seven-level voltages are as follows.

- For an output voltage level $V_{ao}=V_{dc}$, turn on all upper-half switches $S_1.S_2.S_3.S_4.S_5.S_6$ and turn off all lower-half switches $S_1'.S_2'.S_3'.S_4'.S_5'.S_6'$.
- For an output voltage level $V_{ao}=4V_{dc}/6$, turn on upper-half switches $S_2.S_3.S_4.S_5.S_6$ and one lower switches S_1'.
- For an output voltage level $V_{ao}=5V_{dc}/6$, turn on upper-half switches $S_3.S_4.S_5.S_6$ and lower-half switches $S_1'.S_2'$.
- For an output voltage level $V_{ao}=V_{dc}/2$, turn on upper-half switches $S_4.S_5.S_6$ and lower-half switches $S_1'.S_2'.S_3'$.
- For an output voltage level $V_{ao}=V_{dc}/3$, turn on upper-half switches $S_5.S_6$ and lower-half switches $S_1'.S_2'.S_3'.S_4'$.
- For an output voltage level $V_{ao}=V_{dc}/6$, turn on upper-half switch S_6 and lower-half switches $S_1'.S_2'.S_3'.S_4'.S_5'$.
- For an output voltage level $V_{ao}=0$, turn off all upper-half switches $S_1.S_2.S_3.S_4.S_5.S_6$ and turn on all lower-half switches $S_1'.S_2'.S_3'.S_4'.S_5'.S_6'$.

Table.2 Switching states for seven levels DCMI

Output Va0	S_1	S_2	S_3	S_4	S_5	S_6	S_1'	S_2'	S_3'	S_4'	S_5'	S_6'
$V_7=V_{dc}$	1	1	1	1	1	1	0	0	0	0	0	0
$V_6=5V_{dc}/6$	0	1	1	1	1	0	1	0	0	0	0	0
$V_5=4V_{dc}/6$	0	0	1	1	1	1	1	1	0	0	0	0
$V_4=V_{dc}/2$	0	0	0	1	1	1	1	1	1	0	0	0
$V_3=V_{dc}/3$	0	0	0	0	1	1	1	1	1	1	0	0
$V_2=V_{dc}/6$	0	0	0	0	0	1	1	1	1	1	1	0
$V_1=0$	0	0	0	0	0	0	1	1	1	1	1	1

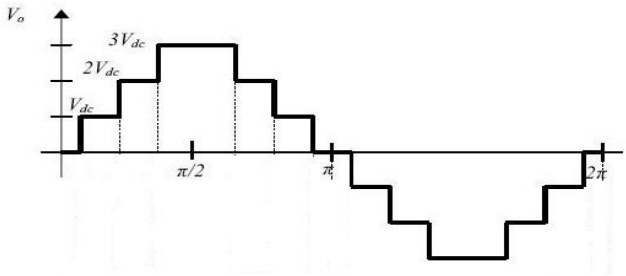

Figure.3 Staircase line voltage waveform of seven level DCMI

Hardware Implementation

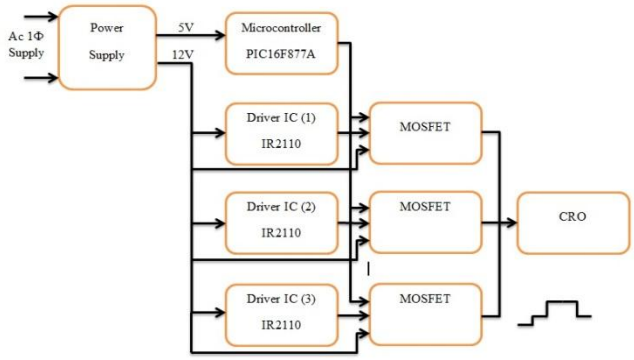

Figure.4 Block Diagram of Hardware

To Capture and Compare the PWM modules aversion of the modulator suitable for the voltage control, accepts as: Inputs the voltage demand in dq stator coordinates (U & U,) and generates the on-line single-phase PWM digital waveforms, which drive the power stages. In the proposed solution, the modulator hardware is just an 8-bit microcontroller with minimum additional logic, which provides the interface with power stage. The microcontroller is a PIC16F877A microcontroller for specially designed for complex, real-time control applications. It shares a common, register-based architecture core that eliminates the accumulator bottleneck and enables fast context switching. Although the 16F877A microcontrollers are 8-bit architecture, all devices have bit, byte, word and 8-bit operations. The motion control family has peripherals that are optimized for single-phase AC induction motor control and power inverter applications. These devices have a unique peripheral, the capture and compare module (CCM), which greatly simplifies the control with 7- level PWM inverter gate driver circuit and external hardware used for generating single-phase pulse width modulation waveforms. The capture and compare carrier-overlapping PWM pulses with resolutions of 250 ns (with a 16 MHz oscillator). Once initialized, the CCM require changing PWM duty. The CCM features programmable Switching (or carrier) frequency up to 1 kHz, duty cycle and dead time. The dead time generator (included in the CCM peripheral) prevents the complementary outputs from being turned on at the same time, in order to avoid a short circuit in one leg of the power inverter. This peripheral also has all programmable high drive capability outputs for each phase. The outputs have programmable polarity, or may be forced high or low. Fig. 3 shows the CCM how to produces the PWM waveforms. The register determines the switching frequency. The CC-COUNTER register is an 8-bit counter which is clocked every state machine. When the counter is running, it continuously counts up and down between. When the counter equals the outputs are complemented, so, this register set the pulse width. Each time the CC-COUNTER register reaches the CCRELOAD value, an interrupt is generated (PI-Interrupt). This interrupt is used to CC-COMP register values (if needed) [2].

- Capture is 16-bit, max. Resolution is 12.5 ns
- Compare is 16-bit, max. Resolution is 200 ns
- PWM max. Resolution is 10-bit

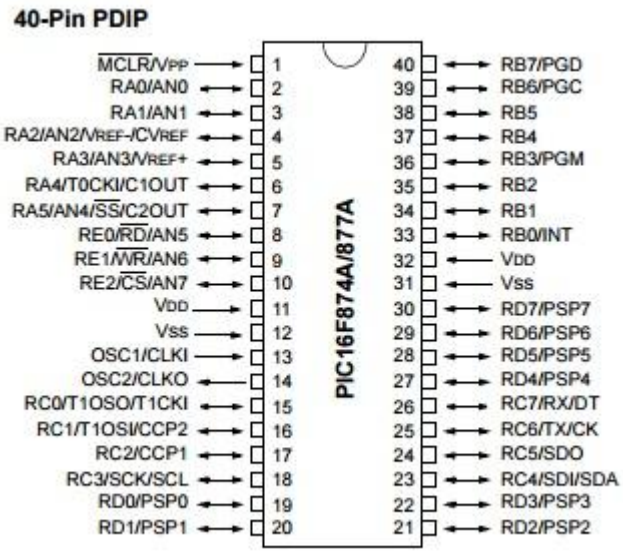

Figure.5 Pin Diagram of Microcontroller (PIC16F77A)

Core features:-

- High-performance RISC CPU
- Only 35 single word instructions to learn.
- All single cycle instructions except for program branches which are two cycle.
- Operating speed: DC - 20 MHz clock input DC – 200 ns instruction cycle.
- Up to 8K x 14 words of Flash Program Memory, Up to 368 x 8 bytes of Data Memory (RAM)
- Up to 256 x 8 bytes of EEPROM data memory

- Interrupt capability (up to 14 internal/external
- Direct, indirect, and relative addressing modes.
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST).
- Programmable code-protection.
- Power saving SLEEP mode.
- Selectable oscillator options.
- Low-power, high-speed CMOS EPROM/EEPROM technology.
- Fully static design.
- In-Circuit Serial Programming (ICSP) via two pins.
- Only single 5V source needed for programming capability..
- Processor read/write access to program memory.
- Wide operating voltage range: 2.5V to 5.5V.
- Commercial and Industrial temperature ranges.
- Low-power consumption

Experimental Results

The performance of proposed control approaches validated with the help of scaled laboratory prototype shown in figure.6 that has system comments as given in table.3

Table.3 System Component and Specification

Sr No.	Name of Component	Specification
1	Micro-controller	PIC 16F877A
2	Diode	IN4001
3	Filter Capacitor	1000µF/100V
4	Voltage Regulator	IC LM7805 & LM7812
5	Supply Transformer	230/12V
6	MOSFET	STP55NF06

This section presents the experimental results of the asymmetric seven-level inverter employing SPWM a technique. PIC16F877A is used to generate trigger pulses for the semiconductor devices (MOSFET) used in the circuit.Which is an optically coupled gate that combines a Gas plight emitting diode. Fig.7 shows the hard ware set-up of diode clamped 7-level inverter for three phase induction motor. Figure.6 shows the experimental setup circuit diagram of seven level diode clamped multilevel inverter and Figure7, shows the staircase sinusoidal line voltage output waveform of seven-level diode clamped multilevel inverter and check on CRO. The hardware and power components run in under operating temperature in normal and industrial environment. Different input voltages are applied to check the motor performance for suitable running with the help of solar power as input source in further uses. Fig.7 shows complete hardware model in below.

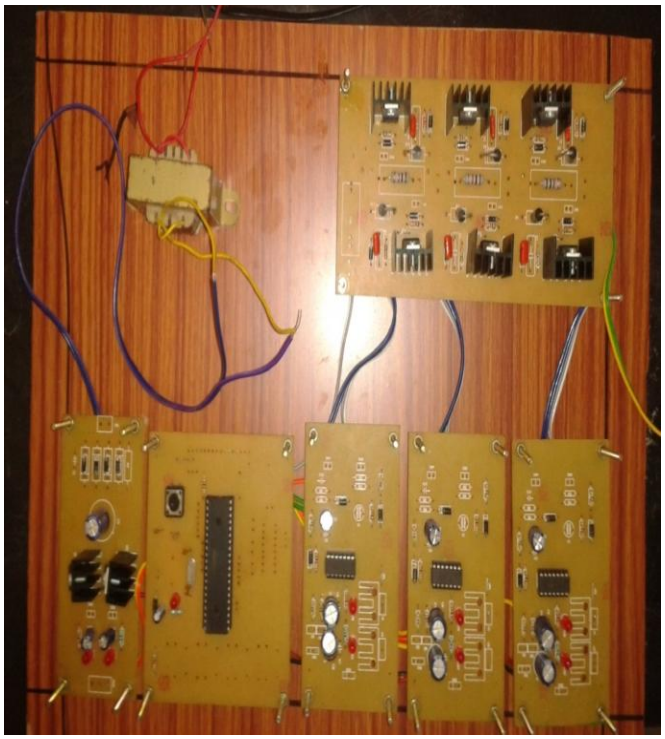

Figure.6 Seven level multilevel inverter Prototype Working Model

AC input (230V, 50Hz) is rectified using a diode rectifier (1N4001). It is filtered using a capacitor filter (1000µF).This filter voltage is applied to the microcontroller (PIC16F877A) and driver IC2110. Microcontroller to generate pluses and applied MOSFET & driver IC drive the MOSFET.MOSFET used for switching purpose .The output of the inverter is fed to the induction motor. Input pulses to the MOSFETs are generated to connected load. The line to line voltages are displayed on CRO, This shown in figure.7

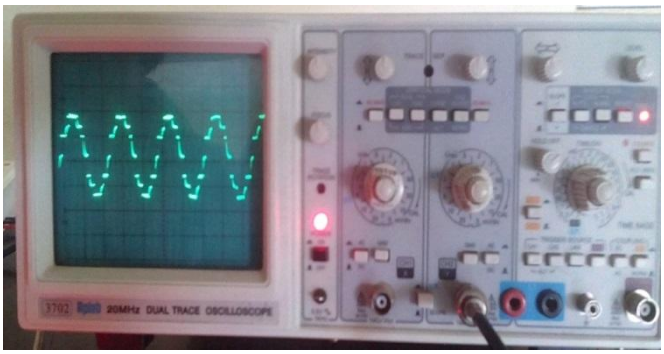

Figure.7 Staircase voltage waveform of seven level diode clamped multilevel inverter

Conclusion

A SPWM technique, suitable for staircase voltage waveform is checked on a CRO. Three phase induction motor fed by an MOSFET 7-level SPWM inverter. The solution is based on a high performance 8- bit microcontroller with gate driver circuit and additional hardware. The implemented algorithm is very efficient, leaving enough time to implement. High switching frequencies can be achieved with fine resolutions within a large output frequency range.

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