Open access Journal International Journal of Emerging Trends in Science and Technology

Low Voltage Low Dropout Regulator with Current Splitting Technique

Authors
Anurag Pise[1], Akash Bhagat[2]
[1]PG Scholar, Yeshwantrao Chavan College of Engineering, RTMNU University, Hingna Road, Nagpur, India
Email: *anuragpise@gmail.com*
[2]PG Scholar, Yeshwantrao Chavan College of Engineering, RTMNU University, Hingna Road, Nagpur, India
Email: *akaii26@gmail.com*

Abstract
Integrated regulators are used for power management in modern portable devices. There are many primary regulators and post regulators which converts high dc voltages, but they are unable to work on low voltage with low quiescent current. A low-voltage low-dropout regulator with current splitting technique is proposed which converts a low-voltage of 1V to an output of 0.6 V with 90 nm CMOS technology. A power noise cancellation mechanism is formed at rail-to-rail output stage of error amplifier (EA) which minimizes the size of power MOS transistor. A transient accelerator (TA) is formed to reuse the part of EA which achieves high current efficiency.

Keywords: *Fast Transient Response, High Power Supply Rejection, Low Dropout (LDO) Regulator, Low Input Voltage*

1. Introduction

As demand rises for electronic devices to be smaller, faster and more efficient, increasing importance is placed on well designed voltage regulators for power supplies. In case of portable devices, space is limited. Therefore, circuitry for multiple functions requires multiple voltage levels on the same chip. Voltage regulators are needed to protect the rest of the circuitry from fluctuations in the power supply, which can occur due to crosstalk or digital switching. Large variations in the power supply are extremely detrimental; voltages that are too high can damage sensitive semiconductor devices, while voltages that are too low may disrupt biasing or even prevent the circuitry from working at all.

2. Previous Work

Low-dropout regulators (LDO) are widely used in electronic products due to their precision output voltage and less prone to noise. In designing of LDOs, stability is an important issue. In some topologies external capacitors are used for the stability of LDOs. These topologies are termed as low drop-out regulators with capacitors. Use of external capacitors provides a good stability on the cost of portability of device. The stability of LDOs can be achieved by some special compensation techniques and topologies without using external capacitors. LDOs without any requirement of external capacitors are termed as capacitor free low drop-out regulators. Main cause of instability in LDOs is due to pass devices. In CMOS low drop-out regulators, usually common-source PMOS pass elements are used, which have high output impedance. Due to high output impedance the output pole location will be changed with the variation in load and in turns low circuit stability. So, there is requirement of some compensation techniques to improve the stability of LDOs.

Adaptive miller compensation (AMC) technique based LDO structure [6] provides high stability, as

well as fast line and load transient responses. This structure also provides good performance on PSRR at high frequency. However, there are some disadvantages with this structure. The gain-band width (GBW) of this LDO is directly proportional to trans-conductance of pass device, which depends on output current, so it is not suitable for large current design. C. K. Chava [7] proposed a low drop-out voltage regulator with low equivalent series resistance (ESR) capacitive loads. In this approach a zero is generated internally by using frequency compensation technique. Due to generation of internal zero there is less dependency on ESR for stability. In frequency compensation approach, this structure utilizes the concept of capacitive feedback. The capacitive feedback introduces a zero in left side of the s-plane. This introduced zero in the feedback loop is used to eliminate the requirement of ESR. It also minimizes the overshoot as it has less requirement of ESR. This structure does not consume significantly higher ground current or chip area compared to conventional low drop-out regulator. The authors have also suggested that the charge pump as voltage booster is an alternative of ESR. The charge pump voltage booster generates a voltage higher than supply voltage and the error amplifier utilizes that voltage for driving a pass device. This structure provides low output impedance, which in return provides stability. This structure has some disadvantage of requirement of additional circuitry. Both these circuits are with capacitor circuits which also increases the area of regulator.

A capacitor free LDO structure with an input current differencing technique to achieve sleep-mode efficiency and area saving has been proposed in [8]. Instead of using an operational amplifier as the error amplification block, it consists of a current differencing (CD) stage. The main advantage of this technique is that it allows low-voltage operation. Also, the configuration renders a smaller feedback factor that reduces the excessive loop gain. Do Couto [9] propose a low drop-out regulator using multi-gate transistors. In this approach, LDO includes a multi-gate transistor at differential stage. First gate of this multi-gate transistor responsible for generating a nominal bias current and second gate is responsible for adjusting the bias voltage based on output. This approach reduces the transients in the regulator output voltage resulting from sudden changes in current drawn by the device load.

3. Proposed Work

The complete voltage regulator design is found in Figure.1. The design has two stage error amplifiers (EA) as stage 1_EATA and stage 2_EA, biasing circuit, a power PMOS transistor and a feedback network.

3.1. Block Diagram representation of proposed LDO

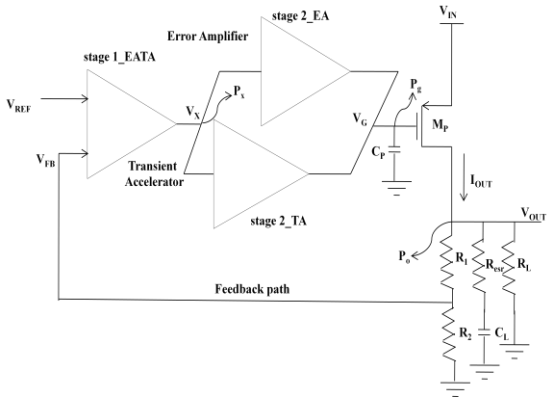

Figure.1. Block Diagram of proposed LDO

A high loop gain is mandatory in LDO regulator design to achieve optimum performance values such as accurate output load regulation and PSR. A low supply voltage and output-resistance reduction induced by a shrinking technology limit the achievable gain of the EA. Thus, there are many auxiliary circuits that consume considerable I_Q that are proposed to enhance performance. A Mp with a significant size is required for a specific load current when an LDO regulator sinks current from a low voltage power source. Thus, the EA requires a higher current slew rate to drive the Mp. To achieve low-voltage operation, an EA with not more than three stacked transistors between the supply voltage and ground is preferred, each of the transistors has more voltage space to stay in the saturation region. A possible candidate can be as simple as an Operational transconductance amplifier (OTA) with a low-cost gain-boosting technique like current splitting. The EA also requires a wide output swing

to minimize the size of the Mp, and hence relieve the requirement on output current slew rate of the EA.

The voltage variation and recovery time during the load current transient is included in the transient response. The voltage variation is more important than the recovery time as even a small output voltage variation (50mV) can cause severe performance degradation to the load circuit operating at an ultralow supply voltage (0.5V). A large closed loop bandwidth of LDO regulator and a large output current slew rate of EA are required to reduce the output voltage variation. However, increase in the closed loop bandwidth may affect the pole/zero location and the circuit becomes too complex consuming more I_Q. Therefore, concept of TA, shown in Figure.2, is adopted to provide extra charging/discharging current paths, depending on the status of output variation detector.

In a Low Voltage LDO regulator design, some performing auxiliary circuit and large Mp occupy considerable space. EA with wide output swing can reduce the size of the Mp. To support a wide load current range (0-100mA) and wide output voltage range (0.5-0.85V), Mp may enter the triode region when under a heavy load condition (large V_{SG}) with a low dropout voltage (small V_{SD}). Therefore, Mp should be large enough to make the intrinsic gain close to the triode region, maintaining high loop gain of LDO regulator.

3.2. Design of Error Amplifier

The simple symmetric OTA as error amplifier (EA) as shown in Figure.2 consists of M_{EA1} –M_{EA9}, where $g_{mi|i=1\text{-}9}$, $r_{oi|i=1\text{-}9}$ and $\lambda_{i|i=1\text{-}9}$ represent the corresponding transconductance, output resistance and the channel length modulation coefficients respectively. The EA does not require compensation capacitor and operates at a minimum supply voltage ($V_{DD,min}$) equal to one threshold voltage plus twice the overdrive voltage $(V_{DD,min} = V_T + 2 \times V_{OV})$ and operate with low supply voltage (≤ 1). The symmetric structure of the EA also has a low input offset voltage for the regulator to achieve an accurate output.

The EA achieves a rail-to-rail output swing at node V_G the output stage (M_{EA7} and M_{EA9}), which can minimize the size of Mp required by a specific load current. Reducing the size of Mp, reduces the circuit area and contributes to a smaller gate capacitance. This allows EA to drive the Mp by a large enough slew rate with relatively low biasing current. The gain of the EA (A_{EAO}) is as follows:

$$\begin{aligned} A_{EA0} &= g_{m2} \times A \times (r_{07} || r_{09}) \\ &\approx g_{m2} \times A \times r_{09} \\ &= \frac{2I_{d2}}{V_{OV2}} \times A \times \frac{1}{A \times I_{d2} \times \lambda_9} \\ &= \frac{2}{V_{OV2} \times \lambda_9} \end{aligned} \quad (1)$$

where we assume $(r_{07} \gg r_{09})$ and let $\{I_{d2}, V_{OV2}, A\}$ represent the bias current, overdrive voltage of M_{EA2}, and current ratio between the first and second stages of the EA respectively. The A_{EAO} in (1) is too low to achieve a fast transient response and high PSR. Therefore, we apply a current splitting technique to boost the gain by maintaining g_{m2} and increasing r_{09}. The transistors M_{gb1} and M_{gb2} can reduce the bias current being mirrored to the second stage of the EA.

Thus, the gain of the modified EA (A_{EAM}) is boosted by a factor of 1/B as follows:

$$\begin{aligned} A_{EAM} &\approx g_{m2} \times A \times r_{09} \\ &= \frac{2I_{d2}}{V_{OV2}} \times A \times \frac{1}{A \times B \times \lambda_9 \times I_{d2}} \\ &= \frac{A_{EAO}}{B} \end{aligned} \quad (2)$$

where B is the splitting ratio and is <1.

The schematic of the proposed LDO is shown on Figure.2. It includes two stage error amplifier (EA), transient accelerator (TA), pass transistor along with capacitive load and Resr.

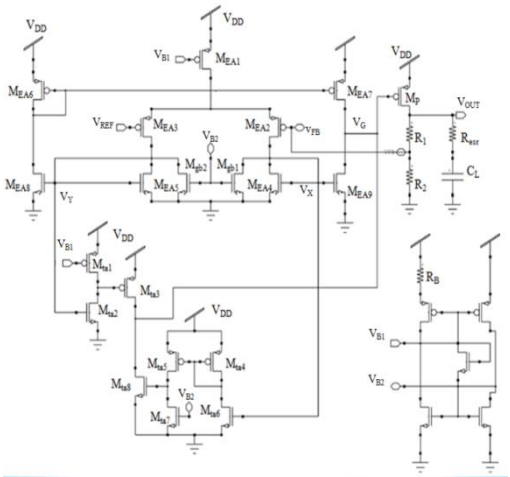

Figure.2. Schematic of LDO regulator

3.3. Design of Low Frequency model of EA and pass transistor

To provide a clean and accurate output voltage with a low voltage level (≤1V), noise suppression is necessary. An n-type power MOS transistor or a cascaded power MOS transistor structure can achieve a high PSR but they are unfeasible for sub 1V operations. Therefore, a p-type power MOS transistor is used with a high loop gain or good noise cancellation at node V_G, which achieve a high PSR. However, it is difficult to achieve a high loop gain with a low supply voltage. In addition the circuit for the power noise cancellation mechanism increases the design complexity and consumes extra I_Q. Thus a concept of resource sharing power noise cancellation mechanism is used as shown in Figure.2.The first stage (stage 1_EATA) of EA attenuates the power noise whereas the second stage (stage 2_EA) of EA rejects the common mode noise (V_{icm}) at its input and creates a replica of supply noise at the output. EA and TA shares stage 1_EATA saving the cost and I_Q.

A p-type device is chosen to construct the power MOS Mp, because of the low supply voltage and low-dropout voltage requirements. The gain-boosted OTA-based EA improves the loop gain of the LDO regulator, which in turn enhances the PSR performance. In addition, we create a replica of the power noise at the gate terminal of the Mp to cancel out the power noise at the source terminal of Mp. This further improves the PSR performance. To reduce the area and I_Q, we use the existing EA to replicate the power noise instead of using an auxiliary circuit. The two equivalent resistors between the output nodes (V_X and V_Y) of the first stage of the EA (stage1_EATA) and the ground have a low resistance value ($1/gm4$ and $1/gm5$); therefore, the power supply noise of stage 1_EATA can be attenuated at nodes V_X and V_Y. Only a small level of power supply noise can be coupled to nodes V_X and V_Y, as they appear in the form of a common mode input to the output stage of the EA (stage 2_EA). This is due to the symmetric structure of stage 1_EATA.

The common mode noise gain of stage 2_EA can be derived using the low-frequency small-signal model shown in Figure.3, with an assumption of $(r_{06} \gg 1/g_{m6})$. We first assume that the power noise is propagated by stage 1_EATA through the common mode signal v_{icm} and causes a fluctuation on v_{g6}. The output v_g induced by v_{icm} is given by,

$$\begin{aligned} v_g &= \left(g_{m7}v_{g6} - g_{m9}v_{icm}\right)\cdot(r_{07}||r_{09}) \\ &\approx \left(g_{m7}\frac{g_{m8}}{g_{m6}}v_{icm} - g_{m9}v_{icm}\right)\cdot \\ &(r_{07}||r_{09}) \\ &= \left(\frac{g_{m7}}{g_{m6}}g_{m8} - g_{m9}\right)v_{icm}\cdot(r_{07}||r_{09}) \\ &\approx 0 \end{aligned} \quad (3)$$

where we assume that M_{EA8} and M_{EA9} are matched devices $(g_{m8} = g_{m9}), (r_{08} \gg 1/g_{m6}) and\ (g_{m6} \approx gm7)$. To cause g_{m6} to be close to g_{m7}, the channel length of M_{EA6} and M_{EA7} are selected to be five times the minimum length to reduce the effect of channel length modulation.

Then, we ground both the nodes V_X and V_Y and input the power noise from the power supply (V_{DD}). The small signal model shown in Figure.3.is used to show how the power noise is replicated to v_g. The result is as shown below:

$$\begin{aligned} v_g &= \frac{r_{09}}{r_{07}+r_{09}}v_{dd} + i_{dd}(r_{07}||r_{09}) \\ &\approx \frac{r_{09}}{r_{07}+r_{09}}v_{dd} + \left(\frac{r_{07}r_{09}}{r_{07}+r_{09}}\right)\frac{v_{dd}}{r_{08}} \\ &\approx v_{dd} \end{aligned} \quad (4)$$

Application of the Superposition theorem by summing (3) and (4), we can conclude that almost the entire power supply noise is replicated to the gate terminal of M_P (v_g) and can be very well seen in Figure.3.

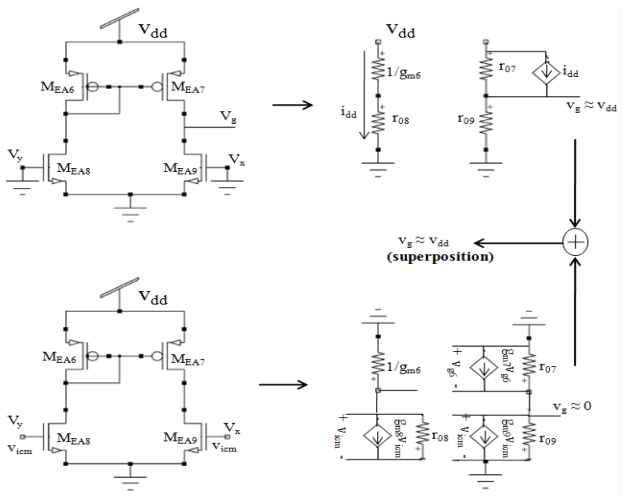

Figure.3. Small signal model of EA output stage for ripple cancellation.

4. Experimental Result

Different analysis can be performed for the proposed schematic such as transient analysis and AC analysis. In transient analysis we are getting the desired output as shown in Figure.4.

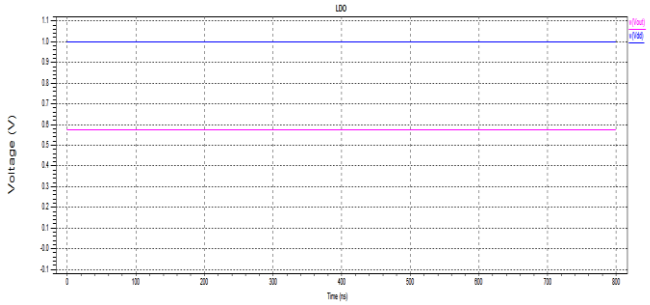

Figure.4. Transient Analysis

When we apply a low input voltage (1V) as an input to our proposed schematic we get 0.6 V as an output voltage. Applying the same input voltage as 1V we are getting different output at different temperature levels as can be seen in Figure.5.

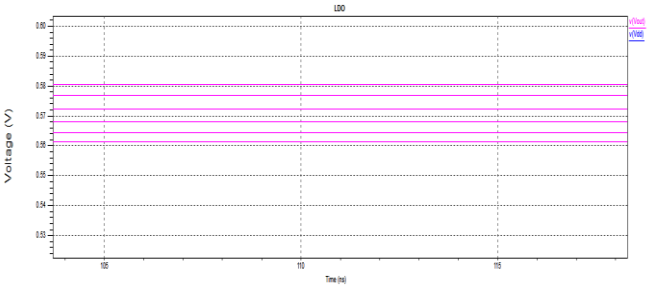

Figure.5. Transient Analysis at different temperature.

There is very less variation in output voltages at different temperature as can be seen from figure.5.

5. Conclusion

In this paper, a CMOS low drop-out regulator with improved PSRR has been developed. The proposed circuit utilizes the current splitting technique for improving the value of PSRR at dc level along with two stage error amplifier with PMOS mirror load, which provides better PSRR bandwidth. The proposed circuit has been simulated using 90nm CMOS technology process parameters and the simulation results have been presented. The proposed circuit provides an output voltage of 0.6V for the low input voltage of 1V.

References

1. Chung Hsun Huang, Ying Ting Ma and Wei Chen Liao, “Design of a Low-Voltage Low-Dropout Regulator”, IEEE Transactions on VLSI Systems, Volume 22, No.6, June 2014.
2. A. P. Patel and G. A. Rincon Mora, “High Power Supply Rejection (PSR) Current-Mode Low-Dropout(LDO) Regulator”, IEEE Transactions on Circuits Systems II, Exp. Briefs, Volume 57, No.11, pp. 868-873, Nov. 2010.
3. M. El Nozahi, A. Amer, J. Torres, K. Entesari and E. Sanchez Sinencio, “High PSR Low Dropout Regulator with Feed-Forward Ripple Cancellation Technique”, IEEE Journal on Solid State Circuits, Volume 45, No.3, pp. 565-577, March 2010.
4. H. C. Lin, H. H. Wu and T. Y. Chang, “An Active Frequency Compensation Scheme for CMOS Low-Dropout Regulators with Transient Response Improvement”, IEEE Transactions on Circuits Systems II, Exp. Briefs, Volume 55, No.9, pp. 853-857, Sep. 2008.
5. J Hu, B. Hu, Y. Fan and M. Ismail, “A 500 nA quiescent, 100 mA Maximum Load CMOS Low-Dropout Regulator”, In Proceedings of the IEEE International Conference on Electronics Circuits Systems, December 2011, pp. 386-389.
6. X. Lai, J. Guo, Z. Sun and J. Xie, “A 3A CMOS Low-Dropout Regulator with Adaptive Miller Compensation”, Analog Integrations on Circuits Signal Process, Volume 49, pp. 5-10, Oct. 2006.
7. C. K. Chava and J. Silva Martinez, “A Frequency Compensation Scheme for LDO Voltage Regulators”, IEEE Transactions on Circuits and Systems I: Regular papers, Volume 51, pp. 1041-1050, June 2004.
8. J. Hu, W. Liu and M. Ismail, “Sleep-mode Ready, Area Efficient Capacitor-free Low-Dropout Regulator with Input Current-differencing”, Analog Integrations on Circuits Signal Process, Volume 63, pp.107-112, Jan. 2010.

9. Do Couto, "Low Dropout Voltage Regulator using Multi-Gate Transistors", U.S. patent 7 928 706, April 2011.
10. Y. Shiyang, Z. Xuecheng, Z. Zhige and C. Xiaofei, "A Loop-improved Capacitor-less Low-Dropout Regulator for SoC Power Management Applications", IEEE Asia-Pacific Conference on Power and Energy Engineering, Volume 10, pp. 1-4, March 2009.
11. W. M. C. Sansen, Analog Design Essentials. New York, NY, USA : Springer Verlag, 2008, Chapter 7.
12. G. A. Rincon Mora, Analog IC Design with Low-Dropout Regulators, New York, NY, USA: McGraw-Hill, 2009, Chapter 1.

Author Profile

Anurag A Pise received the B.E. degree in Electronics and Communication Engineering from Dr. Babasaheb Ambedkar College of Engineering and Research, RTMNU, Maharashtra in 2012. He is currently a M.Tech Scholar at Department of Electronics, Yeshwantrao Chavan College of Engineering, Nagpur.

Akash N Bhagat received the B.E. degree in Electronics and Telecommunication Engineering from Bapurao Deshmukh College of Engineering, RTMNU, Maharashtra in 2011. He is currently a M.Tech Scholar at Department of Electronics, Yeshwantrao Chavan College of Engineering, Nagpur.