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Comparative Study of SiGe MOSFET with Single Substrate MOSFET Using Visual TCAD

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Abstract

A comparative study of SiGe based MOS transistor with single Si and Ge based MOS transistors has been investigated. The objective of this study is to analyze the performance of SiGe MOSFET which shows some significantly better electrical characteristics as compared to the silicon and Germanium channel MOSFET's. Design, Simulation and analysis of transistors has been performed with the help of Visual TCAD.

Keywords: *SiGe, NMOS, Visual TCAD, I-V characteristics.*

INTRODUCTION

According to the predictions of International Technology Roadmap of Semiconductors (ITRS), there is anintensive need for the replacement of the silicon as a substrate material in a nanoscale MOSFET. Germanium, SiGe, III-V materials or Grapheme have been seen as a potential replacement to silicon. This is required because the Moore's law follow in the sub nanoscale technologies. Recently, the global semiconductor industry is seeing a new trend called "More-than-Moore" (MtM), where added values to devices are provided by incorporating functionalities that do not necessarily scale according to Moore's Law.

According to the Moore's Law number of transistors on a chip will double every 18 months. However, Moore's Law will one day face its ultimate limitation, due to the physical properties of the chip. In electronics chip fabrication the key focus are packing more transistors on a chip to provide better performance and power which develops MtM technology on the top of the Moore's Law technologies to provide further values to semiconductor chips.

We know that the vertical and horizontal electric fields seriously affected the mobility in the MOS device at the nanometer scale.. The reduction in the carrier mobility reduces the drain current and eventually the speed of the transistor. The main advantage of using these alternate materials is to increase the carrier mobility in a MOSFET.[1-3]. It is well known that silicon devices dominate the microelectronics industry. It plays 98% of sales in the global semiconductor market, largely because of their low manufacturing cost. However, the driving force behind today's growth in high-speed optical networking and inexpensive, lightweight personal-communications devices is not silicon but silicon–germanium (SiGe).

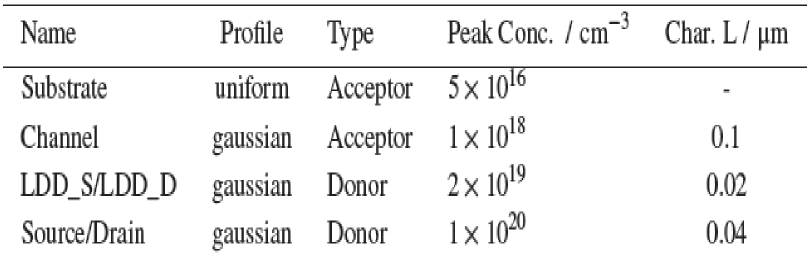
This technology increases operating speed, reduces electronic noise, lowers power consumption, supports higher levels of integration, and, thus, enables the design of more functional components on a chip. SiGeis a revolutionary process technology in which the electrical properties of silicon are improved with germanium to make the chips operate more efficiently. Introducing germanium into the base layer of an otherwise all-silicon bipolar transistor improves operating frequency, current, noise, and power capabilities. It acts a bridge between low-cost, low-power, low-frequency silicon chips and high-cost, high-power, high-frequency made from class III-V semiconductor materials such as gallium arsenide and indium phosphide.

Bell Laboratories discovered that SiGe has a smaller band gap than conventional silicon, making it useful for building transistors that leads the design of heterostructures[4,5]. One of the advantages of SiGe technology that maintains state-of-the-art silicon processing. SiGe processing is relatively simple as compare to high-speed semiconductors made of two or more materials because silicon and germanium have similar chemical and physical properties. Ordinary silicon does not operate at frequencies above a few gigahertz, so it has drawback to use in higher-speed wireless telecommunications devices. In contrast to silicon-based chips, SiGe semiconductors provide higher speed.[6]

SiGe or silicon-germanium, is a general term for the alloy $Si_{1-x}Ge_x$ which consists of any molar ratio of silicon and germanium.

DESIGN AND SIMULATION

The general processes to design 180nm MOSFET involving simulation of fabrication process, structure and mesh and electrical testing. the first step for designing the MOSFET is to draw the ‘device drawing’ using VisaulTCAD , further meshing is done. The doping profiles used in the the designed MOSFET is listed as bellow[7] :



Name	Profile	Type	Peak Conc. / cm^{-3}	Char. L / µm
Substrate	uniform	Acceptor	5×10^{16}	-
Channel	gaussian	Acceptor	1×10^{18}	0.1
LDD_S/LDD_D	gaussian	Donor	2×10^{19}	0.02
Source/Drain	gaussian	Donor	1×10^{20}	0.04

The designed structure of MOSFET and the material used in structure are shown in fig 5 and 6

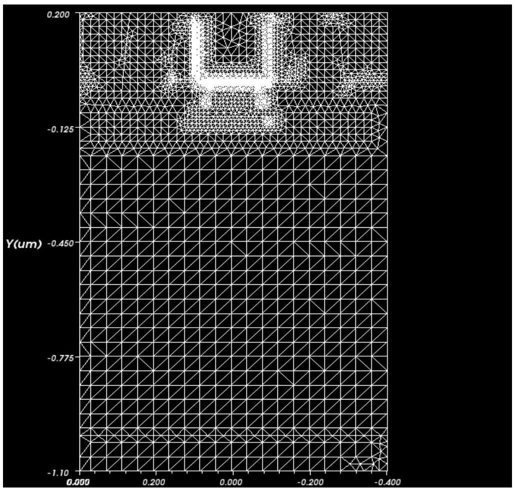


Figure 1: Mesh structure of MOSFET

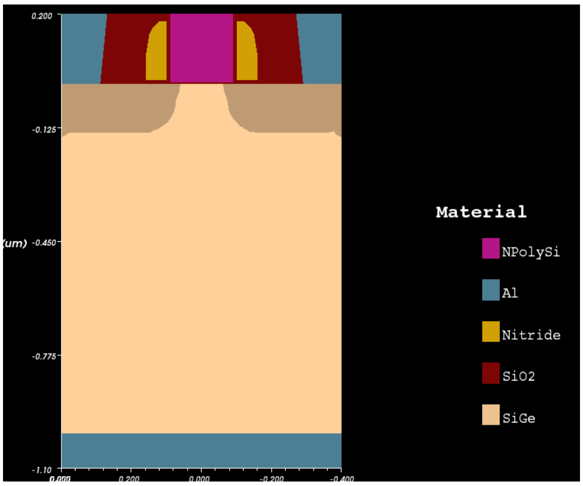


Figure 2: Basic Structure of MOSFET with

RESULT AND ANALYSIS

We have analyzed and simulated the output drain current of Si, Ge base MOSFET and SiGe MOSFET for variable mole fraction ($Si_{1-x}Ge_x$ MOSFET). The Simulated result are as follows : (x represent the mole fraction of germanium in the result)

Table 1: Drain Current of Si/Ge MOSFET and SiGe with different mole fraction at fix gate voltage

Drain Voltage	Drain current for x=0.3	Drain current for x=0.5	Drain current for Ge based MOSFET	Drain current for Si based MOSFET	Drain current for x=0.9	Drain current for x=0.7
0	5.28E-17	1.61E-17	-1.79E-17	-1.92E-16	8.36E-17	1.17E-16
0.2	0.00032134	0.00032557	0.00028934	0.0003137	0.00033088	0.00032989
0.4	0.000565	0.00057384	0.00049552	0.00054992	0.00058416	0.00058227
0.6	0.00070853	0.00072224	0.00060212	0.00068657	0.0007372	0.00073447
0.8	0.00076522	0.00078245	0.00063786	0.00073882	0.0008005	0.00079721
1	0.00078208	0.00080033	0.00065181	0.00075449	0.00081927	0.0008158
1.2	0.0007909	0.00080921	0.00066148	0.00076305	0.00082832	0.00082483
1.4	0.00079781	0.00081597	0.00066951	0.00076988	0.0008351	0.00083161
1.6	0.0008038	0.00082174	0.00067659	0.00077586	0.00084087	0.00083737
1.8	0.00080919	0.00082693	0.000683	0.00078129	0.00084602	0.00084253
2	0.00081414	0.00083168	0.0006889	0.00078627	0.00085073	0.00084725

Table 2: Drain Current of Si/Ge MOSFET and SiGe with different mole fraction at fix drain voltage

Gate Voltage	Drain current for Ge based MOSFET	Drain current for Ge based MOSFET2	Drain current for x =0.9	Drain current for x= 0.7	Drain current for x = 0.5	Drain current for x = 0.3
0	1.07E-11	7.28E-12	1.52E-09	1.12E-09	8.45E-05	6.77E-11
0.2	3.10E-10	2.19E-09	2.11E-07	1.65E-07	0.00018231	1.53E-08
0.4	3.84E-08	6.18E-07	1.10E-05	9.85E-06	0.00030162	2.67E-06
0.6	3.72E-06	2.19E-05	5.91E-05	5.67E-05	0.00043237	3.61E-05
0.8	3.86E-05	8.49E-05	0.00013643	0.00013346	0.00056966	0.0001063
1	0.00010836	0.00017288	0.00023113	0.0002279	0.00071089	0.00019756
1.2	0.00019863	0.0002753	0.00033701	0.00033364	0.00085487	0.00030159
1.4	0.00030149	0.00038702	0.00045058	0.00044714	0.00100078	0.00041414
1.6	0.00041279	0.00050522	0.00056972	0.00056625	0.00114815	0.00053273
1.8	0.00053009	0.00062813	0.00069298	0.0006895	0.00129663	0.00065577
2	0.00065181	0.00075449	0.00081927	0.0008158	0.00144598	0.00078208

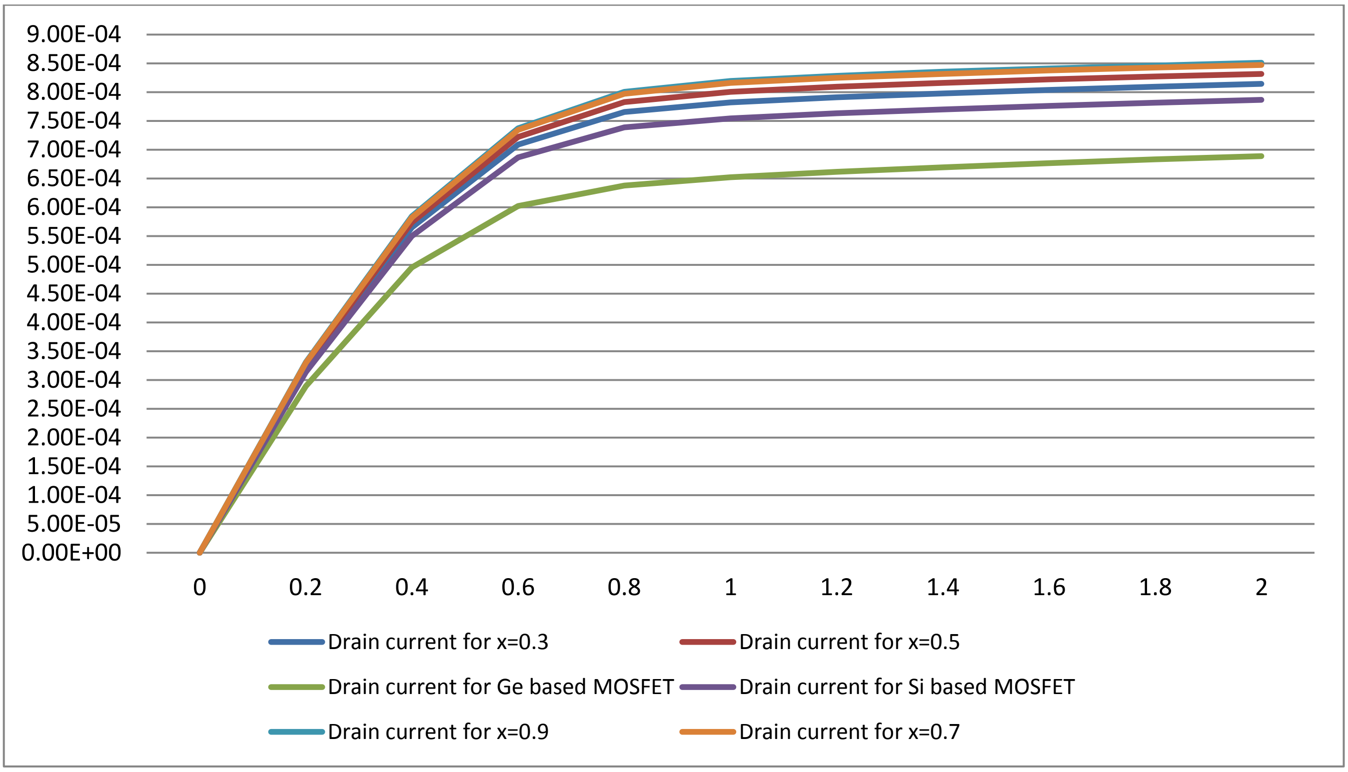


Figure 3 : Comparison drain characteristics curve of designed MOSFETs

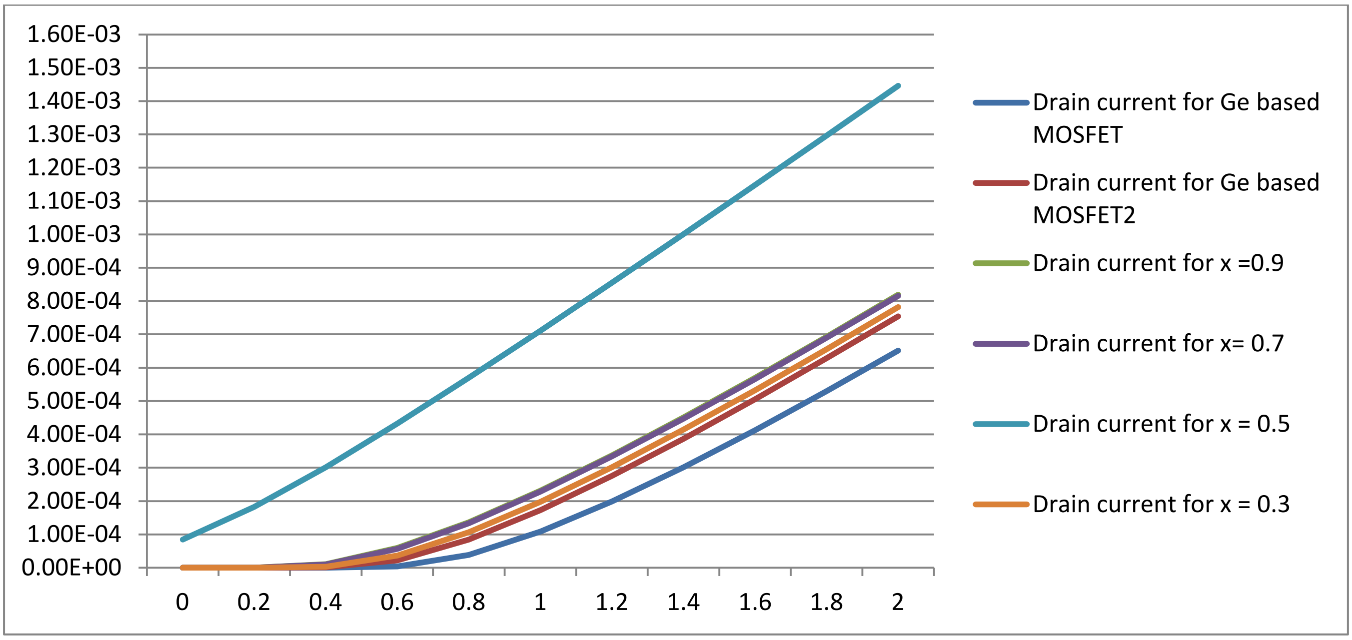


Figure 3 : Comparison transfer characteristics curve of designed MOSFETs

From the simulated result we can see that for different value of mole fraction of SiGe the darin current is higher than the Si and Ge base MOS transistor.

CONCLUSION

The effect of mole fraction of SiGe on the characteristic curve of drain-source current verse gate voltage/ drain voltage in designed SiGe MOSFETs has been studied. By varying the mole fraction of SiGe without altering other parameters the drain current value is noted. From the above simulation we can conclude that designed SiGe MOSFET provide better drain and transfer characteristics in comparison of Si and Ge base MOS transistors..

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