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Design and Implementation of 4-bit Pipeline ADC using 0.09µm CMOS Technology

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Abstract
This paper focuses on design and implementation of 1.1V, 4-bit Pipeline Analog to Digital Converter [ADC]. The ADC consists of sample and hold, latched comparator and summing circuit and amplifier of gain 2. The ADC has been designed and simulated in standard gpdk90ηm CMOS technology library using Cadence tool.

Keywords: ADC, CMOS, gpdk90ηm.

1. Introduction

An Analog-to-Digital converter is a device, which translates an analog voltage signal into a corresponding digital number. Whenever we relate to the real world most of the signals are analog in nature. But some applications such as digital signal processing requires signals to be digital. In such situations it becomes necessary to get analog to digital conversion using an ADC. Analog-to-digital converter is a fundamental block in mixed-signal VLSI circuits [1]. ADC is the key components in communication and video system. With development of these electronics system, high resolution and high-speed ADCs are becoming more and more important. High-speed low-power Analog-to-Digital converters (ADCs) are the critical building blocks for modern communication and signal processing systems. They are the interface between the analog and digital signal processing. Since the mid-1970s, ADCs have been widely designed using integrating, successive approximation, flash, and delta-sigma techniques. More recently, there has appeared a new class of ADC with an architecture known as pipeline, which offered an attractive combination of high speed, high resolution, low power dissipation and small die size [2].The pipeline ADC, therefore, became the optimum solution for present low power applications, such as a wireless communication system. A continued search for circuit architectures and techniques enabling ADCs to obtain higher speed and resolution with smaller chip area and lower power dissipation, therefore, is necessary. Pipeline analog-to-digital converters represent the majority of the ADC market for medium- to high-resolution ADC.

2. Block Diagram of Pipeline ADC

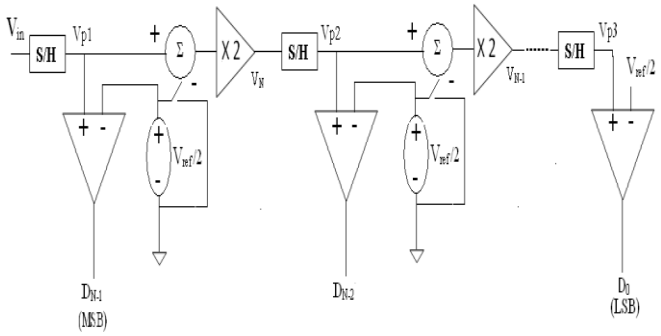

Figure 1: N-bit Pipeline ADC architecture

Fig.1 shows a typical pipeline ADC is an N-step converter, with 1 bit being converted per stage. The pipeline ADC consists of N stages connected in series .Each stage contains a 1-bit ADC (a comparator), a sample-and-hold, a summing circuit, and amplifier of gain 2. Each stage of the converter performs the following operation:

1. After the input signal has been sampled, compare it to $V_{ref}/2$. The output of each comparator is the bit conversion for that stage.
2. If $V_{in} > V_{ref}/2$(comparator output is 1), $V_{ref}/2$ is subtracted from the held signal and pass the result to the amplifier. If $V_{in} < V_{ref}/2$ (comparator output is 0), then pass the original input signal to the amplifier. The output of each stage in the converter is referred to as the residue.
3. Multiply the result of residue by 2 and pass the result to the next stage.

1. Sample and Hold: The function of the S/H circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing. The simplest S/H circuit in CMOS technology is shown in Fig 2. Where V_{in} is the input signal, M1 is an MOS transistor operating as the sampling switch, Ch is the hold capacitor, clk is the clock signal, and Vout is the resulting sample-and-hold output signal.

2. Latched Comparator: The comparator is the most important component in the ADC architecture. When the input signal voltage is less than the reference voltage, the comparator output is at logic '0'.when the input signal voltage is higher than the reference voltage, the comparator output is at logic '1'.

3. Amplifier of gain 2: Amplifiers have the ability to increase the magnitude of an input signal, it is useful to be able to rate an amplifier's amplifying ability in terms of an output/input ratio. The technical term for an amplifier's output/input magnitude ratio is *gain*. As a ratio of equal units (power out / power in, voltage out / voltage in, or current out / current in), gain is naturally a unitless measurement [9].

3. Design and Simulation

The design analysis of Pipeline ADC is done in terms of schematic simulation.

1. Sample and Hold

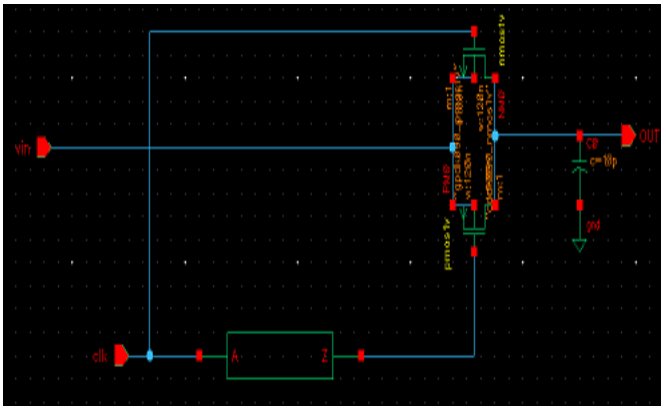

Figure 2: Sample and HoldFig. 2 shows Sample and Hold circuit that samples the voltage of a continuously varying analog signal and holds its value at a constant level for a specified minimal period of time 0.025µs. The sample time is 0.05µsec , amplitude is 100mV to -100mV, total time period for one cycle is 0.325µsec & frequency is 3.076 MHz. Sample and Hold circuit consists of each nmos & pmos of width 120ηm and length 100ηm, 10pico farad capacitor and 1-input NOT gate.

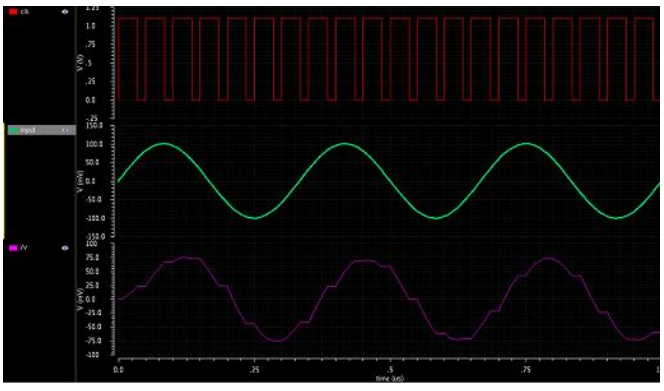

Figure 3: Transient response for Sample and Hold

2. Latched Comparator

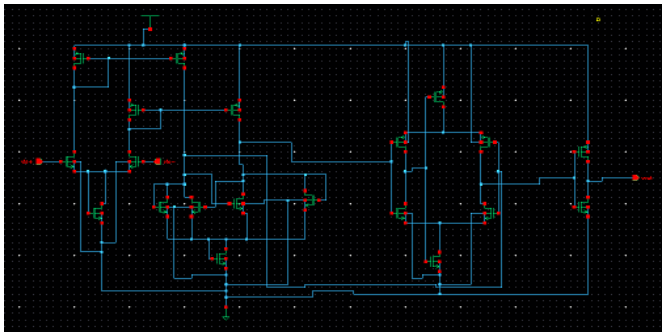

Figure 4: Latched Comparator

The input stage differential amplifier the gain of this stage is rather low (because of the diode connected PMOS load M3-M4)); the low node impedance ensures high speed (high bandwidth) operation. The fully differential output ensures rejection of the common mode component of the input signal. The current mirrors (M6-M7) acting on the fully differential output of the first stage, can be used to impart a current gain (by choosing a suitable W/L ratio). The diode connected NMOS pair M8-M9, acts as low impedance load for this stage. The other NMOS pair (M10-M11) with cross connected gates act as normal logic inverters forming a latch – the decision circuit.

The inverters pair forming the latch need to have a voltage gain larger than unity. Considering the fact that the diode connected MOS (M8-M9) act as the load on these inverters, the sizing of M10-M11 should be such as to ensure the inverter gain to be larger than unity. The output of the latch may require shaping, to be compatible with logic circuits. This is usually done with the help of an amplifier. In the present case a single ended differential amplifier is used for this purpose. However, since the input excursion to this differential amplifier is limited, the latch output may require a level shifter to meet this requirement. The diode connected MOS M12 acts as a level shifter DC bias. Note that the net current flowing through M12 is a constant (independent of signal conditions).

In the event the comparator needs to drive a heavy load, the single ended differential amplifier output may be fed to a buffer stage (cascaded pair of inverters). The comparator is the most important component in the ADC architecture. Its role is to convert an input voltage (V_{in}) into logic `1' or `0' by comparing a reference voltage (Vref) with the V_{in}. If V_{in} is greater than Vref, the output of the comparator is `1', otherwise `0'. [9]

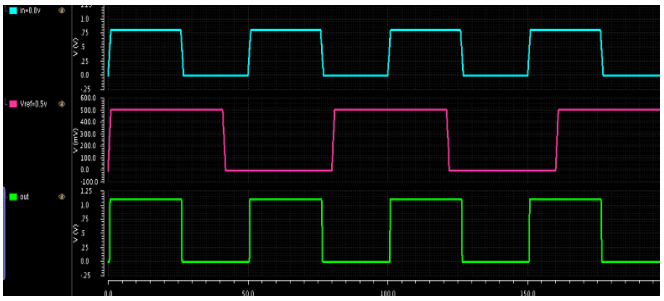

Figure 5: Transient response of Comparator

Fig.5 when the input signal voltage is less than the reference voltage, the comparator output is at logic '0'.When the input signal voltage is higher than the reference voltage; the comparator output is at logic '1'.

4. Amplifier of gain 2

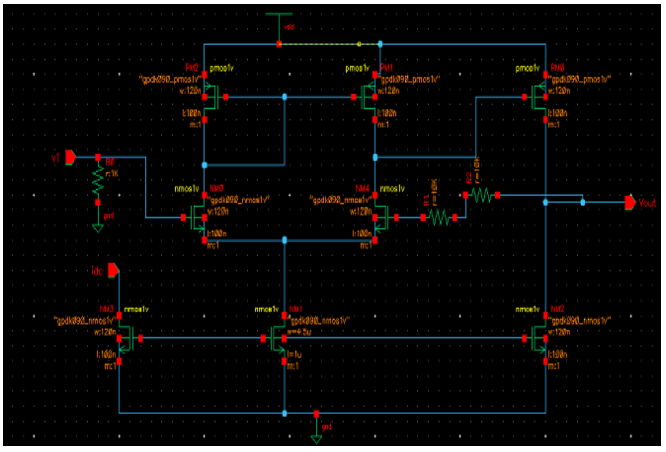

Figure 6: Amplifier of gain 2

A typical CMOS differential amplifier stage is shown in Fig 6. Differential amplifiers are often desired as the first stage with high gain and second stage which provide maximum swing. The first stage generally a differential stage but the second stage is typically design as a simple common source stage so it allows maximum output swing.

In this circuit, feedback resistor R_f (R_1) is of 10kΩ, R_0 is of 10kΩ and R_2 is of 1kΩ. Therefore, $V_0=V_{in}$ (1+ (R_f / R_0)), since the voltage gain is positive, hence the output signal is non-inverted w.r.t the input signal. Here, the closed loop gain is A_f=(1+ (R_f / R_0). This means the gain of the non-inverting amplifier can be changed by changing values of R_f & R_0.

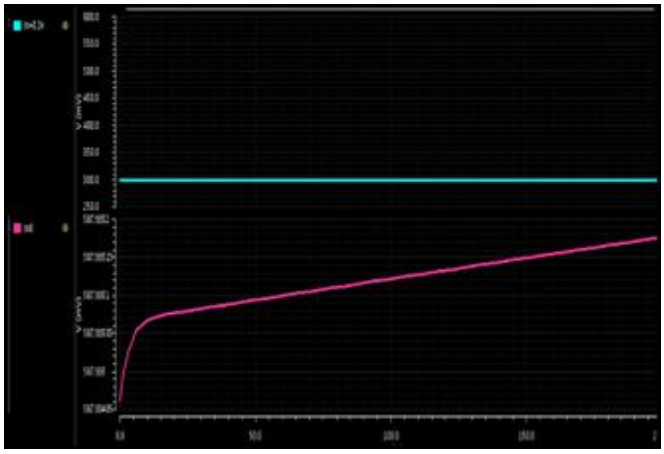

***Figure 7**: Transient response for Amplifier of gain 2*

For example, V_{in}=0.3V, V_{ref}/2=0.5V, here V_{in} < V_{ref}/2 so the held signal directly pass to the gain amplifier circuit and its multiply by 2 i.e., the output value will be Vout = 0.6V. If V_{in} = 0.7V, V_{ref}/2=0.5V, here V_{in} > V_{ref}/2 so the held signal will get subtract with V_{ref}/2 value i.e., the value will be 0.4V & it gets multiply by 2 i.e., the output value will be V_{out}=0.8V.

5. Experimental Results

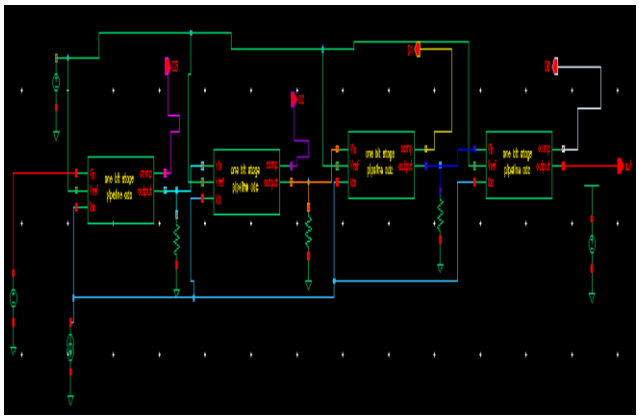

Figure 8: 4-bit Pipeline ADC schematic design

The schematic of 4 bit Pipeline ADC is designed on Cadence tool having gpdk 90ηm as a technology library which is as shown in the Fig 8.Here V_{dc}=1.1V supply is used

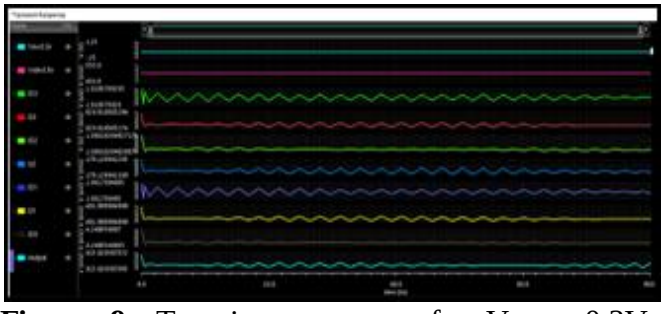

Figure 9: Transient response for V_{in} = 0.3V, V_{ref}=0.5V, digital output will be 0100

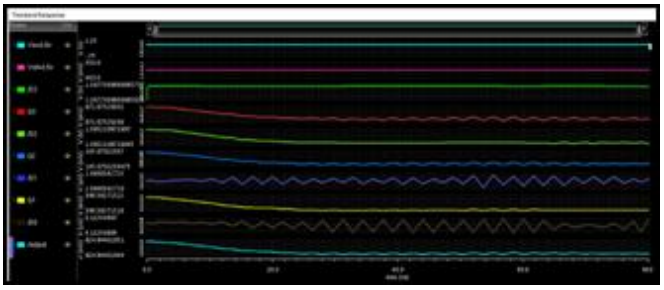

Figure 10: Transient response for V_{in} = 0.8V, V_{ref}=0.5V, digital output will be 1100

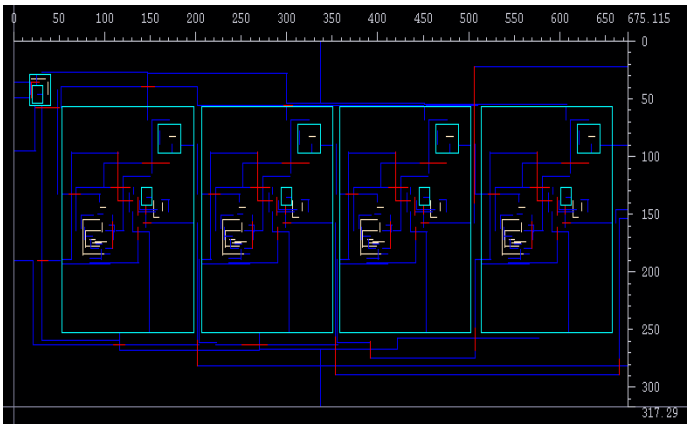

Figure 11: Layout design of 4-bit pipeline ADC

Calculated Area is 675.115ηm x 317.29ηm = 214207.2384(ηm)^2

TABLE I: Summary

Technology	90ηm gpdk
Analog voltage, Vin	1.1v
Reference voltage, Vref	0.5v
Vdd	1.1v
comparators	4
Input Range (Dynamic ra	20*log(2^n-1) = 20*log(2^4 23.52 ≈ 24dB
Resolution	4-bits
SNR	6.02n+1.76dB = 6.02*4+ = 25.84dB
Power Dissipation	0.295m watt
Delay	451.9η sec
Speed	2.2M Samples/S

6. Conclusions

The schematic and layout of sample and hold circuit, latched based comparator, amplifier gain by 2 is designed and integrated. The integrated pipeline ADC is operated at 4-bit precision with analog input voltage of 0 to 1.1V, supply voltage 1.1V, Resolution 4bits, SNR 25.84dB, consumes

0.295m watt power, speed is 2.2M Samples/S and layout Area is 675.115ηm x 317.29ηm = 214207.2384(ηm)^2. The ADC is designed and implemented in standard gpdk90nm CMOS technology of version–IC 6.1.5 (Higher Version) using Cadence virtuoso tool.

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Author Profile

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