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Design and implementation of 4-bit Vedic Multiplier

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ABSTRACT
Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in the early twentieth century from ancient Indian sculptures (Vedas). This paper proposes the design of high speed Vedic Multiplier using the techniques of Vedic Mathematics that have been modified to improve performance .The need of high speed multiplier is increasing as the need of high speed processors are increasing . A Multiplier is one of the key hardware blocks in most fast processing system which is not only a high delay block but also a major source of power dissipation. A conventional processor requires substantially more hardware resources and processing time in the multiplication operation, rather than addition and subtraction.
Keywords- *Vedic Multiplication, Urdhva Tiryakbhyam Sutra, Array Multiplier, CMOS, T-Spice v13.0 (Tanner Tools)*

INTRODUCTION

Multipliers are extensively used in Microprocessors, DSP and Communication applications. For higher order Multiplications, a huge number of adders are to be used to perform the partial product addition. The need of low power and high speed Multiplier is increasing as the need of high speed processors are increasing. The Vedic multiplication technique is based on 16 Vedic sutras or aphorisms, which are actually word formulae describing natural ways of solving a whole range of mathematical problems [1]. The mathematical operations using, Vedic Method are very fast and requires less hardware, this can be used to improve the computational speed of processors. This paper describes the design and implementation of 4x4 bit Vedic multiplier based on Urdhva- Tiryakbhyam sutra (Vertically and Crosswise technique) of Vedic Mathematics using EDA (Electronic Design Automation) tool. The use of Vedic mathematics lies in the fact that it reduces the typical calculations in conventional mathematics to very simple ones. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Vedic Mathematics is a methodology of arithmetic rules that allow more efficient speed implementation. It also provides some effective algorithms which can be applied to various branches of engineering such as computing [2].

1.1 Vertically & Crosswise Technique

The proposed Vedic multiplier is based on the "Urdhv Tiryakbhyam" sutra (algorithm). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same

ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. It is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise" [7]. It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other conventional multipliers.

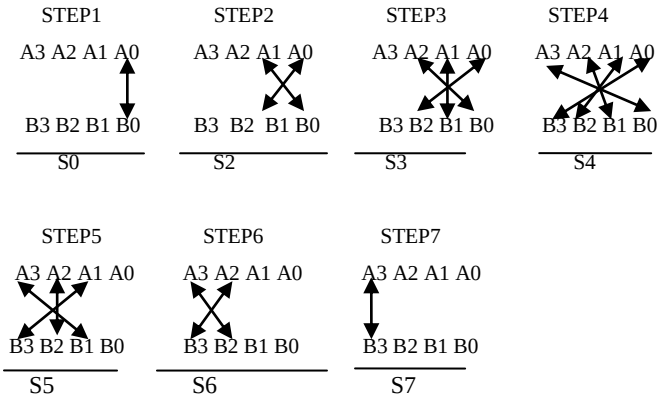

Fig. 1 Vertically & Crosswise Technique

Step1: S0 = A0*B0
Step2: S1 = A1*B0+A0*B1
Step3:S2 = A2*B0+A0*B2+A1*B1
Step4:S3 = A3*B0+A0*B3+A2*B1+A1*B2
Step5:S4 = A3*B1+A1*B3+A2*B2
Step6:S5 = A3*B2+A2*B3
Step7:S6 = A3*B3

Finally the output is : S0S1S2S3S4S5S6

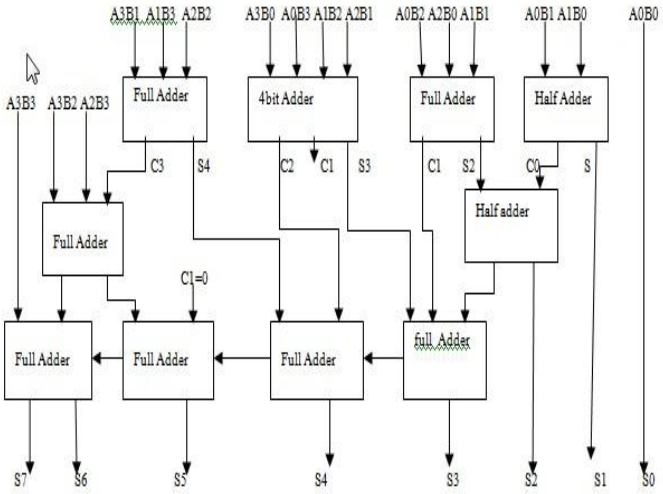

Fig. 2 Block diagram of 4-bit Vedic Multiplier

1.2 Array multiplication

An array multiplier is very regular in structure as shown in fig. 3. It uses short wires that go from one full adder to adjacent full adders horizontally, vertically or diagonally [3]. An n × n array of AND gates can compute all the *i i a b* terms simultaneously. The terms are summed by an array of "n [n - 2]"full adders and „n" half adders. The shifting of partial products for their proper alignment is performed by simple routing and does not require any logic. The number of rows in array multiplier denotes length of the multiplier and width of each row denotes width of multiplicand. The output of each row of adders acts as input to the next row of adders. Each row of full adders or 3:2 compressors adds a partial product to the partial sum, generating a new partial sum and a sequence of carries.

```
                                A3 A2 A1 A0
                              ×B3 B2 B1 B0
                          A3B0 A2B0 A1B0 A0B0
                     A3B1 A2B1 A1B1 A0B1  +
                A3B2 A2B2 A1B2 A0B2  +
           A3B3 A2B3 A1B3 A0B3  +
P7  P6   P5   P4   P3   P2   P1   P0
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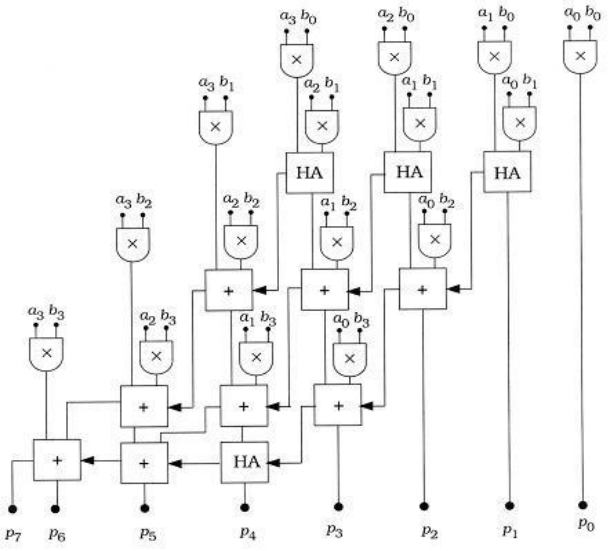

Fig 3 Block diagram of 4-bit Array Multiplier

The delay associated with the array multiplier is the time taken by the signals to propagate through the AND gates and adders that form the multiplication array. Delay of an array multiplier depends only upon the depth of the array not on the partial product width. The delay of the array multiplier is given by [4]:

$(T\ critical) = [(N-1) + (N-2)]*T(Carry) + (N-1)*T(Sum) + T(AND)$

ere T (*Carry*) is the propagation delay between input and output carry, T (*Sum*) is the delay between the input carry and sum bit of the full adder, T (*AND*) is the delay of AND gate, N is the length of multiplier operand.

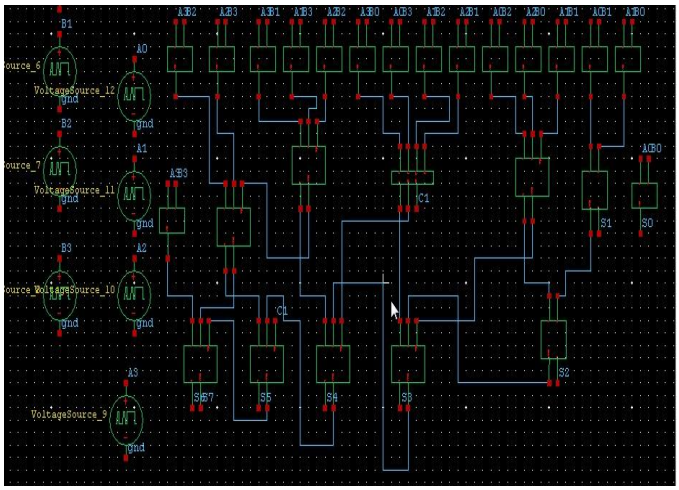

Fig. 4 Implementation of 4*4 Vedic multiplier using CMOS logic

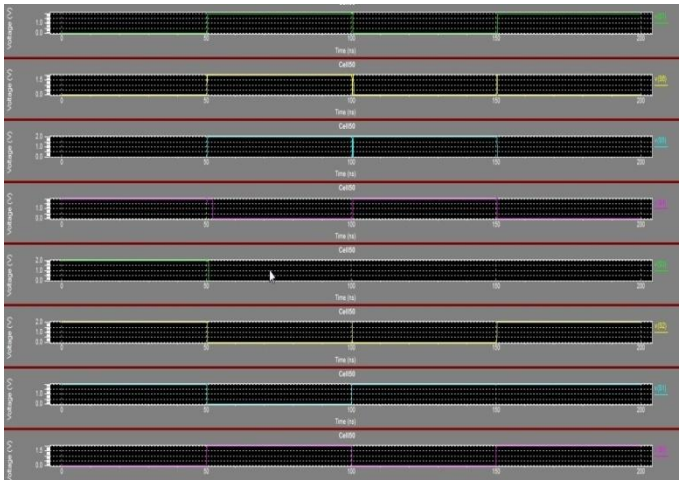

Fig. 5 Waveform of 4*4 Vedic multiplier using CMOS logic

PERFORMANCE PARAMETERS AND SIMULATION SET-UP

The 4*4 bit Vedic multiplier is compared based on the performance parameters like propagation delay, average power consumed, and number of transistor. To achieve better performance, the circuits were designed using CMOS logic process compare 4*4 Vedic multiplier with array multiplier in term of propagation delay, average power consumed ana power delay product. All the circuits have been designed using TANNER EDA with Model file as **dual.md** [6]. The power estimation is a difficult task because of its dependency on various parameters and has received a lot of attention. Direct Simulation method is used in order to analyse the result [5].

Table. No 1

Logic Styles	Delay(ns)	Average power consumed (mW)	Power Delay product (pJ)
Array multiplier(CMOS)	25.3	0.0606	1.533
Vedic Multiplier(CMOS)	0.400	1.62	0.648

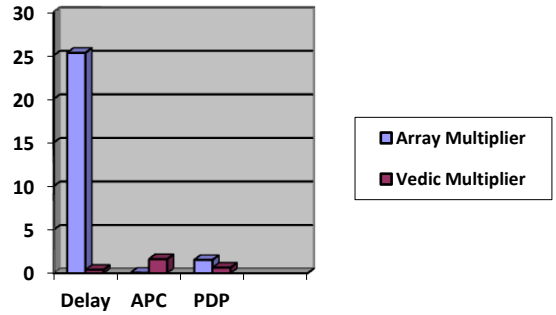

Fig 8 comparison with 4*4 Vedic multiplier using CMOS compared with Array multiplier in terms of delay ,power and power delay product

RESULT ANALYSIS

It has been observed that 4*4 Vedic multiplier is better than 4*4 Array Multiplier. It helps a person to solve problems faster. It provides one line answer. Time saved can be used to answer more questions. It better in terms of Propagation Delay, Average Power Consumed and Power Delay Product(PDP). In terms of propagation delay in Vedic multiplier by using CMOS logic styles is 0.40ns and In Array multiplier Propagation Delay is 25.3ns.As a conclusion 4*4 Vedic Multiplier is better than Array multiplier in terms of Propagation Delay i.e. fastest circuit operation.

CONCLUSIONS

This paper presents a multiplication "Urdhva Tiryakbhyam" Sutra based on Vedic Mathematics. The design of the 4x4 bit Vedic multiplier is Implemented on T-Spice v13.0. It is a method for hierarchical multiplier design which clearly indicates the computational advantages offered by Vedic methods. Using CMOS logic computational path delay is found to be 0.40ns but for multiplier using conventional method (Array) computational path delay is found to be 25.3ns. Hence it can be concluded that the performance of the 4x4 bit Vedic multiplier seems to be highly efficient in terms of speed when compared to Array multipliers. Reducing the time delay is very essential requirement for many applications and Vedic Multiplication technique is very much suitable for this purpose.

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