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Design of Low Power Transversal FIR Filter For VLSI Signal Processing Applications

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Abstract
An efficient novel technique of synthesis of a low arithmetic complexity, linear phase low pass FIR filter is proposed .The output response is modeled using trigonometric functions of frequency and its slopes. This approach has the advantages of ease of computation of the impulse response and reduction in the Gibb's phenomenon. The synthesized filter proves to be a good alternative to the existing FIR filters. This paper deals with the design of 16-tap FIR filter and proposed work has been done using Xilinx ISE 9.2i evaluating the performance by the synthesis report and shown the synthesizes RTL schematic along with the simulation results.

Keywords: *FIR, Transversal, VHDL, Digital Signal Processing, VLSI Signal Processing.*

1. Introduction

Depending on the response of the system, digital filters can be categorized as: Finite impulse response (FIR) and Infinite Impulse Response (IIR) filters Although FIR filters, mainly require higher no. of taps than IIR filters to obtain similar frequency characteristics.FIR filters have linear phase characteristics which guarantees stability and are easy to implement with multipliers, adders and delay elements, so they are extensively used. The number of taps in digital filters varies according to applications. . In commercial filter chips with the fixed number of taps, zero coefficients are loaded to registers for unused taps and unnecessary calculations have to be performed. To diminish this problem, the FIR filter chips provide variable-length taps that can be widely used in many application fields. However, these FIR filter chips use memory, an address generation unit, and a module unit to access memory in an efficient manner. Since the proposed architecture only requires several Multipliers, registers, and adders, the number of gates can be reduced significantly than existing chips. In, general, FIR filtering is described by a simple convolution operation as expressed in the equation

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$$y(k)= \sum_{k=0}^{N-1} h(k).x(n-k)$$

Where x[n] represent data input, y[n] represent filtering output, and h[n] represent a coefficient, respectively and ***N*** is the filter order.

Advantages of FIR OVER IIR

FIR can be designed with exact linear phase.FIR filters are always stable with quantized coefficient. It can be realized in both recursive and non-recursive structures. When FIR filters are implemented on finite–word length digital system they give free limit cycle oscillations The above benefits makes FIR filters attractive enough to be implemented onto a large no. of system. For frequency response, FIR filters have higher order than IIR filters making FIR filters expensive.

2. Related work

Achinta Roy(2014)[3] proposed a technique of generic n-tap Fir filter, the thesis was proposed on design and structure and occupied silicon space, needed for Implementing in fpga the result was full configurable using generic parameters.

Yan Sun and Min Sik Kim [5] presented an approach to implement a high-performance 8-tap digital FIR (Finite Impulse Response) filter using the Logarithmic Number System realize a fast FIR filter by utilizing the Logarithmic Number System, which allows a simple implementation of multiplication using a fixed-point adder.

Fábio Fabian Daitx, 2008 [4] This work proposes an VHDL generation software for optimized FIR filters. In this paper a near optimum algorithm for constant coefficient FIR filters was used. This algorithm uses general coefficient representation for the optimal sharing of partial products in Multiple Constants Multiplications (MCM). The developed tool was compared to Matlab FDA toolbox.

Abul Fazal Reyas Sarwar, Saifur Rahman [2] provided the principles of Distributed Arithmetic, and introduce it into the FIR filters design, and then presents a n-Tap FIR low-pass filter using Distributed Arithmetic. The implementation of FIR filters on FPGA based on traditional method costs considerable hardware resources, which goes against the decrease of circuit scale and the increase of system speed.

Deepshikha Bharti , K. Anusudha [7] ,High speed Finite Impulse Response filter (FIR) is designed using the concept of faithfully rounded truncated multiplier and parallel prefix adder. A transposed form of FIR filter is implemented using an improved version of truncated multiplier and parallel prefix adder. Multiplication and addition is frequently required in Digital Signal Processing.

3.FIR Filter-VHDL

3.1 Traversal Filter

The most commonly used structure in implementing adaptive filters is the traversal structure. the traversal can be divited into two main parts the filter part and update part. the filter output is calculated as a linear combination of the input sequence x(n-k)=0,1…N-1 composeed of delayed samples of x(k). The traversal filter structure is, therefore, a linear temporal filter that processes the temporal samples of its input signal x(k) to produce modified output y(k)

An N-Tap transversal was assumed as the basis for this adaptive filter. Practical considerations are made to determine the value of N. An FIR filter was chosen because of its stability. The use of the transversal structure allows relatively straight forward construction of the filter.

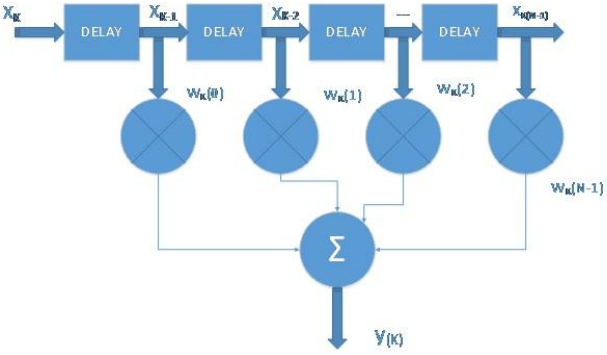

Fig 1: Transverse FIR filter.

As the input, coefficients and output of the filter are all assumed to be complex valued, and then the natural choice for the property measurement is the modulus, or instantaneous amplitude. If y(k) is the complex valued filter output, then amplitude is denoted by |y(k)|.

When the envelope has the proper value the error p(k) will be zero, otherwise non-zero. The error carries sign information to indicate which direction the envelope is in error. The adaptive algorithm is defined by specifying a performance/cost/fitness function based on the error p(k) and then developing a procedure that adjusts the filter impulse response so as to minimize or maximize that performance function.

3.2 VHDL Design Flow Of Traversal FIR Filter

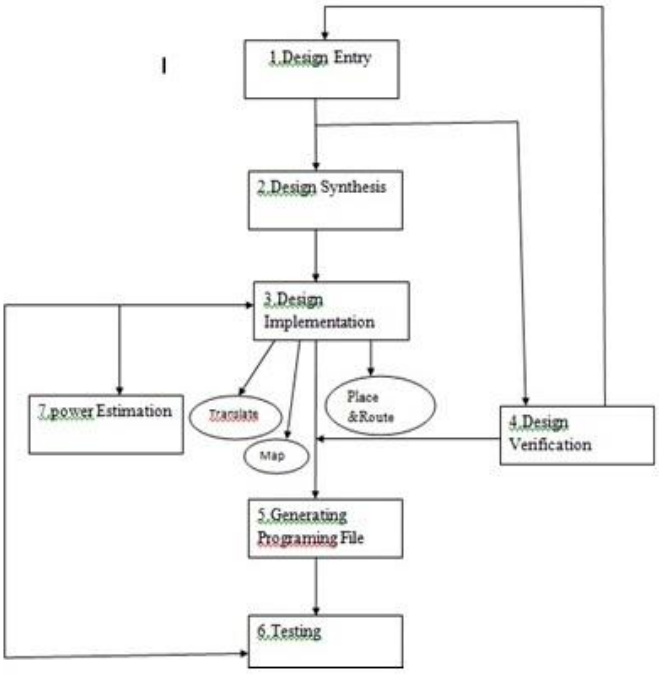

Fig 2: VHDL Flow of Transversal FIR filter design

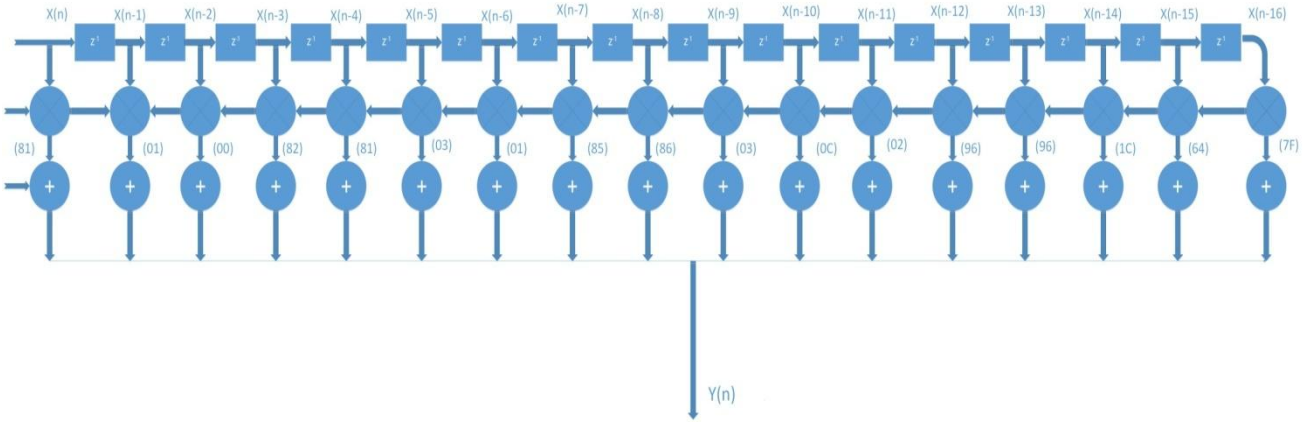

Fig 3: Architectural Diagram

4. Result Analysis

The FIR filter has two basic structures: direct form and transpose form. The direct form has one huge addition at the end as shown in fig 1.The above figure shows that the output of the FIR filter is obtained by performing the multiplication of individual delay line with their respective filter coefficients.

In our proposed method we have synthesized the FIR filter successfully using the ISE tool, the simulation results has been given below showing satisfactory output.

Synthesis

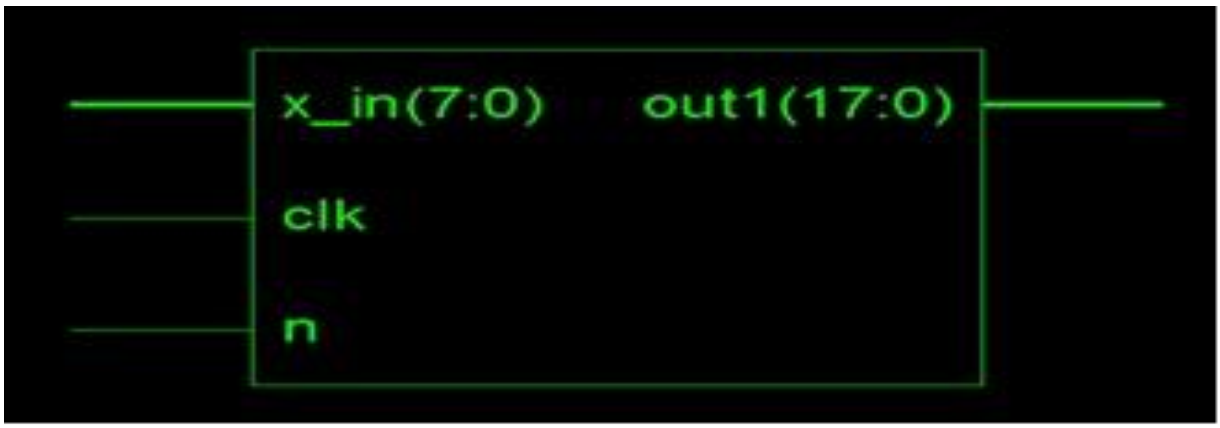

Fig 4: Block diagram of 16-Tap FIR filter.

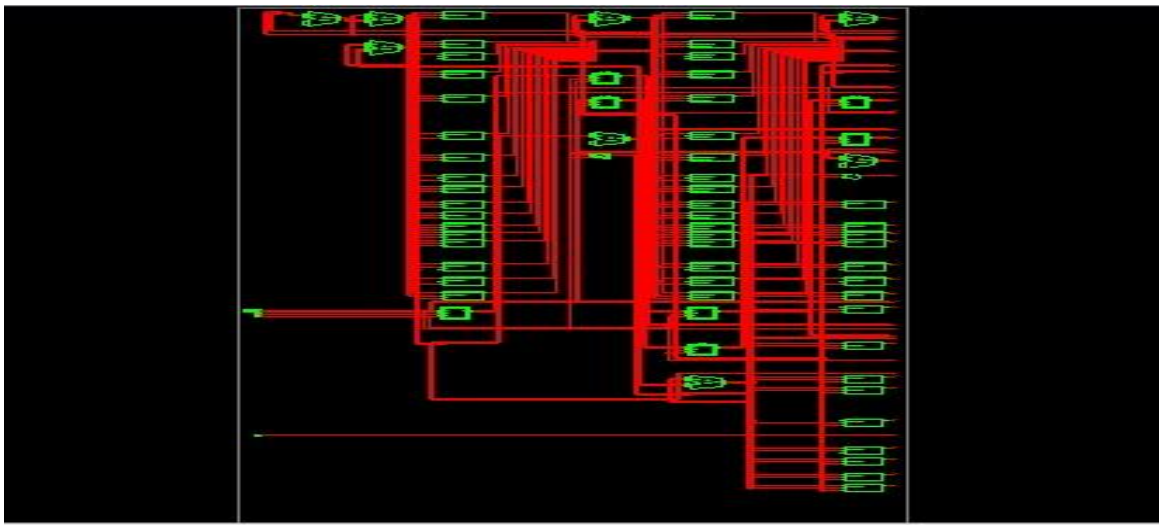

Fig 5: RTL schematic of 16-Tap FIR filter

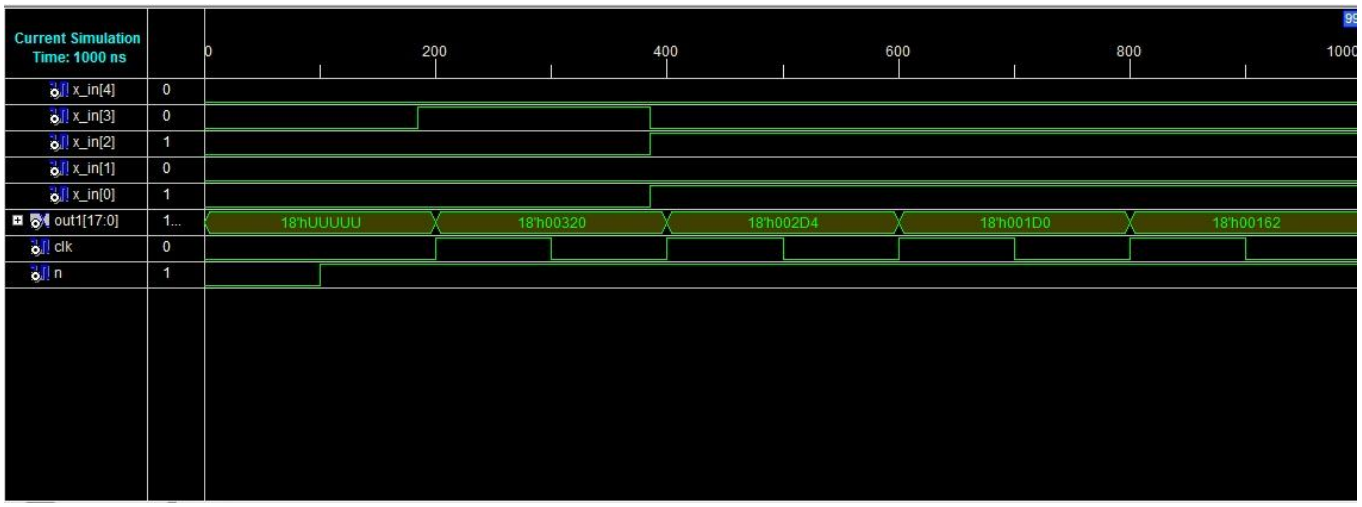

Fig 6: Simulation Result

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	458	768	59%
Number of Slice Flip Flops	260	1536	16%
Number of 4 input LUTs	805	1536	52%
Number of bonded IOBs	28	124	22%
Number of MULT18X18s	4	4	100%
Number of GCLKs	1	8	12%

Fig 7: Device Utilization Summary

Filter Equation

Y[n]=81 X[n] + 1 X[n-1] + 82 X[n-3] + 81 X[n-4] + 3 X[n-5] + 1 X[n-6] + 85X[n-7] +86 X[n-8] + 3 X[n-9] + 12 X[n-10] + 2 X[n-11] +96 X[n-12] + 96 X[n-13] + 1C X[n-14] + 64 X[n-15] + 7f X[n-16]

FILTER COEFFICIENTS

x"8 1"	x"0 1"	x"0 0"	x"8 2"	x"8 1"	x"0 3"	x"0 1"	x"8 5"	x"8 6"	x"0 3"	x"0 c"	x"0 2"	x"9 6"	x"9 6"	x"1 c"	x"6 4"	x"7 f"

FILTER LENGTH = 17

AS WE HAVE ONE TAP EQUAL TO ZERO,TOTAL NO. OF NON-ZERO TAPS=16

THE ORDER OF AN FIR FILTER =16

Power Summary	
Optimization Data	None Production
Quiescent(W)	0.032
Dynamic (W)	0.003
Total (W)	0.035

Fig 8: Power Summary

Voltage Source Information

Source	Voltage	Power (W)	Icc (A)	Iccq (A)
V_{CCINT}	1.2	0.013	0.003	0.008
V_{CCAUX}	2.5	0.020	0.000	0.008
V_{CCO} 3.3	3.3	0.000	0.000	0.000
V_{CCO} 2.5	2.5	0.002	0.000	0.001
V_{CCO} 1.8	1.8	0.000	0.000	0.000
V_{CCO} 1.5	1.5	0.000	0.000	0.000
V_{CCO} 1.2	1.2	0.000	0.000	0.000

Fig 9: Voltage Source Information

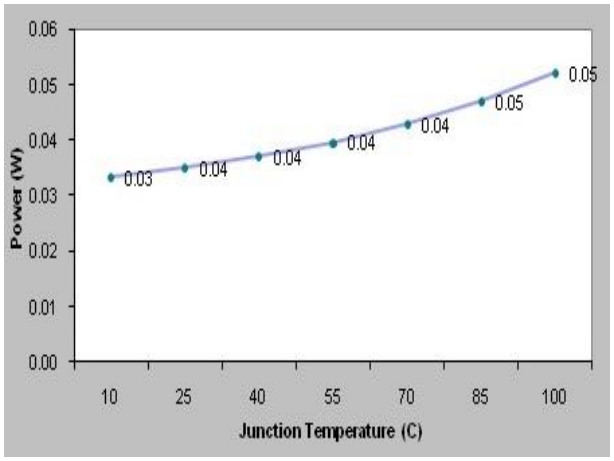

Fig 10: power Vs Temp.

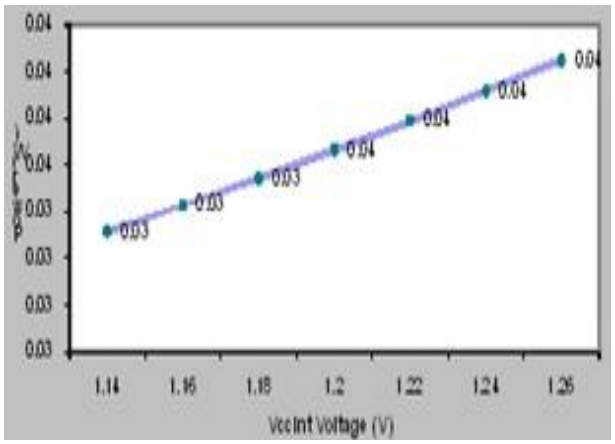

Fig 11: Power Vs Voltage.

5. Conclusion

This paper presents a traversal FIR filter system Algorithm which has flexibility, power-efficiency and configuration time advantages. This project includes ripple carry adder and multiplier with its regular and parallel structure which can be realized easily on silicon as well leads to a reduction in hardware cost. The FIR filter is coded using VHDL and further it is Synthesized using the tool Xilinx9.2i and simulation is done using ISE Simulator.The presented FIR filter system is responsible for providing the best solution for realization and autonomous adaptation of FIR filters, and can be used in many communication and Digital signal processing applications like Channel Equalization, Adaptive noise cancellation, Adaptive echo cancellation, System identification and many others.

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Author Profile

Ms. Soumee Sharmeela Pattnaik perusing M.Tech from Centurion University Of Technology & Management and Completed B.Tech from Krupajal Engineering College in the year 2013.

Mr. Ritisnigdha Das was born on 9th july, 1982. He received the B.Tech degree in Applied electronics and Instrumentation engineering from ITER under Biju pattanaik university and Technology in 2007 and M.Tech degree in Vlsi and Embedded design from centre for microelectronics, CET (BPUT), Odisha in 2010.Currently he is working as Asst. Professor at Centurion University of Technology and management , Bhubaneswar, Odisha. He has also 4 years of teaching experience in Electronics and communication engineering.
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